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THESIS

FIELD-EFFECT TRANSISTOR REACTANCE CIRCUITS

by

Gary Dale Clark

September 1968

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FIELD-EFFECT TRANSISTOR
REACTANCE CIRCUITS

by

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Captain, United States Marine Corps
B.S., University of Oklahoma, 1962

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
September 1968

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ABSTRACT

Efforts to miniaturize the reactance circuits of vacuum-tube technology by using junction transistors have been only partially successful. Large equivalent inductances and capacitances are obtainable, but the effective Q is limited to low values by the low input impedance of these devices. Unipolar field-effect transistors offering high gain and high input impedance are investigated for this application. Analytical models, based on the equivalent circuit of the FET, are developed for reactance circuits employing R-C feedback networks. A simple capacitive reactance circuit, utilizing a first-order feedback network and operating at a frequency of 250 Khz, yielded a low-Q effective capacitance but served to verify the model employed. Computer-aided design of a reactance circuit employing a second-order feedback network resulted in a stable effective capacitance offering Q multiplication. Sensitivity of the feedback voltage to component tolerances precludes packaging this circuit in integrated form, but the feasibility of designing an FET reactance circuit to meet rather precise specifications is demonstrated.

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I. INTRODUCTION

Electronic circuits that draw a leading or a lagging current, known as "Reactance Circuits", are well known in vacuum-tube technology.[1] They are employed for frequency modulation, automatic frequency control, frequency-shift keying, and as variable elements in adjustable filters.[2] The reactance presented to a dynamic circuit may be regarded as an equivalent inductance or capacitance, the value of which depends not only on the circuit parameters but also upon the gain of the tube employed. If the gain, or more specifically the transconductance g_m, of the tube is controlled by a voltage, the circuit then exhibits a voltage-variable reactance.

Efforts to develop similar reactance circuits using junction transistors have met with only partial success. They have been employed for automatic frequency control[3] and frequency modulation[4] of oscillators at audio and slightly higher frequencies. Work performed by Schulz and reported by Dill[5] shows that the effective Q of the "Reactance Transistor" is always low because of the low input impedance of the junction transistor, thus limiting it to applications where considerable loss can be tolerated.

It has been suggested by Newell[6] that the development of field-effect transistors with high gain and high input impedance, might make the reactance transistor feasible. Although such devices have been available for several years, it appears that virtually no work has been done towards implementing them in reactance circuits. It seems important in view of the development of integrated circuitry, that a careful analysis of such circuits be undertaken. Their eventual if not indeed immediate use in packaged devices warrants such an investigation.

This paper is a report of the theoretical and experimental investigation of certain transistor reactance circuits employing field-effect transistors.

II. REACTANCE CIRCUITS

A. Concept

A reactance circuit is dynamic in the sense that it employs feedback of such a nature as to cause it to draw a leading or a lagging, out-of-phase current when an a.c. voltage is applied. In Figure 1, the applied voltage v is shifted in phase and reduced in magnitude by the feedback network β, and applied to the input of the amplifier. The amplifier is characterized by a complex gain, $\overline{A}$, so that the current i is out of phase with the applied voltage. If by proper arrangement of the loop gain $\overline{A\beta}$, the current i lags the applied voltage, the circuit represents an effective inductance, while if the current leads, it represents an effective capacitance. The magnitude of the equivalent inductance or capacitance may be controlled by varying the magnitude of the amplifier gain.

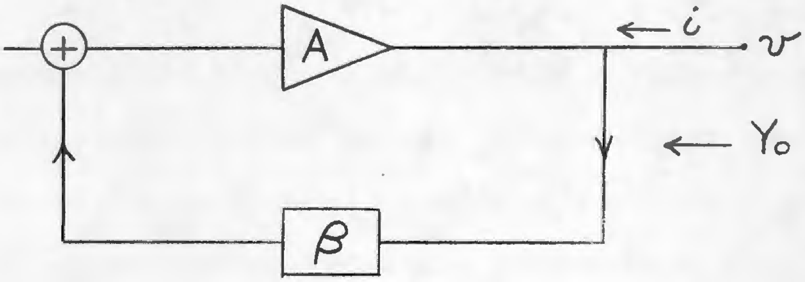


Figure 1. Reactance circuit.

Associated with the out-of-phase, reactive component of current, there is of course an in-phase, resistive component. The relative magnitudes of these two current components determine what is generally known as the quality factor Q of the inductance, or the dissipation factor D of the capacitance. These two quantities are related by definition, and for simplicity in this paper, Q will be associated with both the inductive and the capacitive circuits, where for the capacitive circuits, Q is the reciprocal of D. An ideal reactance would draw no in-phase component of current and it is theoretically possible to so adjust the loop gain of this reactance circuit that the in-phase component of the total current is either positive, zero or negative. In the experimental results reported in this paper, these conditions will be noted.

The equivalent output admittance of the circuit, Y_o, is given by (1), where Y_o' is the output admittance of the amplifier. If the equivalent conductance G_o is zero, then Y_o is a pure susceptance and an ideal reactance has been

$$Y_o = \frac{Y_o'}{1 + \overline{A\beta}} = G_o + jB_o \tag{1}$$

achieved. If G_o is greater than zero, the Q is given by the ratio of B_o to G_o, but if G_o is less than zero the circuit becomes unstable and oscillations will result. Therefore, if high-Q, stable reactances are to be realized, tight phase tolerances are required for the loop gain $\overline{A\beta}$.

B. FET Characteristics[7]

An accurate analysis of the equivalent admittance offered by a reactance circuit must include knowledge of the output admittance of the amplifier, which in turn requires that a correct model be chosen for the device employed. The unipolar field-effect transistors used in these circuits can be represented by the model shown in Figure 2.

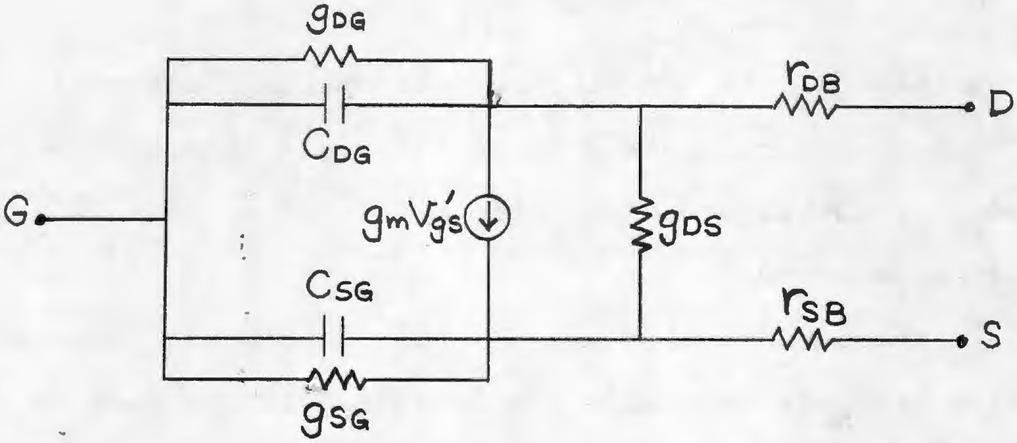


Figure 2. FET equivalent lumped-element model.

FET channel current actually flows in a non-linear distributed R-C transmission line, but for low frequency work it is sufficient to treat the device as if it were a lumped, non-linear electrical network. Capacitances C_{DG} and C_{SG} and conductances g_{DG} and g_{SG} are a lumped-element representation of the reverse-biased gate-to-channel diode. In a well designed FET, g_{DG} and g_{SG} will be quite small and can be considered open circuits. Values r_{DB} and r_{SB} are the bulk resistances of the semiconductor path from the channel edges to the drain and source contacts respectively. These will be in order of 100 ohms or less, depending somewhat on the geometry and manufacturing process. At low frequencies, the effect of r_{DB} is quite negligible and it can be considered as only a very small part of any practical load resistance. The value of r_{SB} has a slight effect on the apparent transconductance of the device; the voltage v'_{gs} in Figure 2 is related to the terminal voltage v_{gs} by

$$v'_{gs} = \frac{v_{gs}}{1 + g_m r_{SB}} \tag{2}$$

The value g_{DS} is the slope of the output characteristics in the inch-off region and is usually less than 50 micro-mhos; however rather broad variations in similar devices are often observed.

These quantities are all bias dependent. The variation of g_m is desirable and necessary if the gain of the device is to be voltage-variable. The dependance of g_{DS} on bias is predicted from the characteristic curves and does not complicate the design provided that the proper operating range is selected. The variations of the diode capacitances, C_{DG} and C_{SG}, with bias are somewhat complex and may prove troublesome in circuits where these capacitances are significant.

At frequencies of interest in this report, conductances g_{DG} and g_{SG} and resistances r_{DB} and r_{SB} can be ignored. Also the value of the transconductance that will be available is the apparent g_m as determined experimentally, thus eliminating the requirement for equation (2). The simplified FET model to be used for analysis is shown in Figure 3.

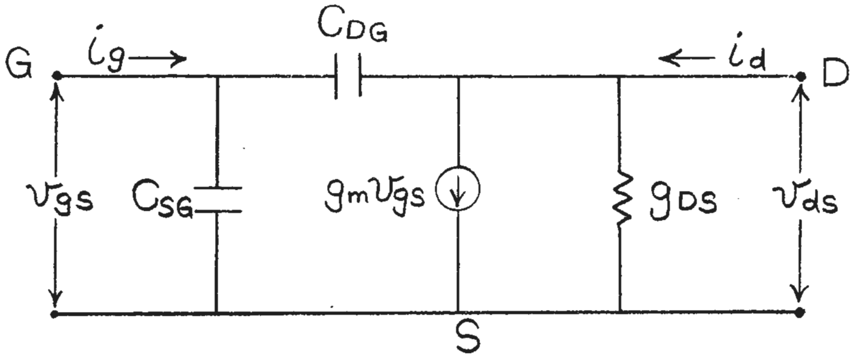


Figure 3. Simplified FET model.

It is common practice among manufacturers to specify the FET by its equivalent short-circuit admittance parameters, referred to the common-source connection. The parametric equations of this network are:

$$i_g = y_{is}v_{gs} + y_{rs}v_{ds} \tag{3}$$

$$i_d = y_{fs}v_{gs} + y_{os}v_{ds} \tag{4}$$

Applying these equations to the physical equivalent circuit of Figure 3, the y parameters obtained are:

$$y_{is} = j\omega(C_{DG} + C_{SG}) \tag{5}$$

$$y_{rs} = -j\omega C_{DG} \tag{6}$$

$$y_{fs} = g_m - j\omega C_{DG} \tag{7}$$

$$y_{os} = g_{DS} + j\omega C_{DG} \tag{8}$$

Since y_{is} and y_{rs} are almost pure capacitances, specification sheets often list equivalent values of C_{iss} and C_{rss} respectively.

Although an analysis can be carried out using the y parameters, it was preferred in this report to reconstruct the equivalent lumped-element model and work directly with it.

C. Simple FET Reactance Circuits

1. General. The similarity between the characteristics of a field-effect transistor and those of a pentode vacuum tube, suggests that known reactance-tube circuits might be adapted to employ FETs. The simplest such reactance circuits consist of a single amplifier with a first-order R-C or R-L phase-shift network as a feedback path.[2] A representative circuit which provides an inductive reactance is shown in Figure 4(a). C_2, C_3, R_g and the choke serve to properly bias the FET, and it is assumed, at least for now, that values can be chosen for these elements such that they have negligible effect on the circuit at the frequencies of interest. The dynamic equivalent of this circuit is shown in Figure 4(b). A capacitive reactance can be obtained by simply interchanging R_1 and C_1 in this circuit.

Resistor and inductor combinations can also be used to provide the appropriate feedback for obtaining equivalent inductive or capacitive reactances; however, they are not widely used in reactance circuits and will not be considered in this report for two reasons. First, inductors with their associated distributed capacitance are susceptible to spurious responses and coupling effects which are to be avoided. Secondly, high-Q inductors are not consistent in size with other integrated components, and to use them would rule out any possibility of producing a reactance circuit which could be packaged in integrated form.

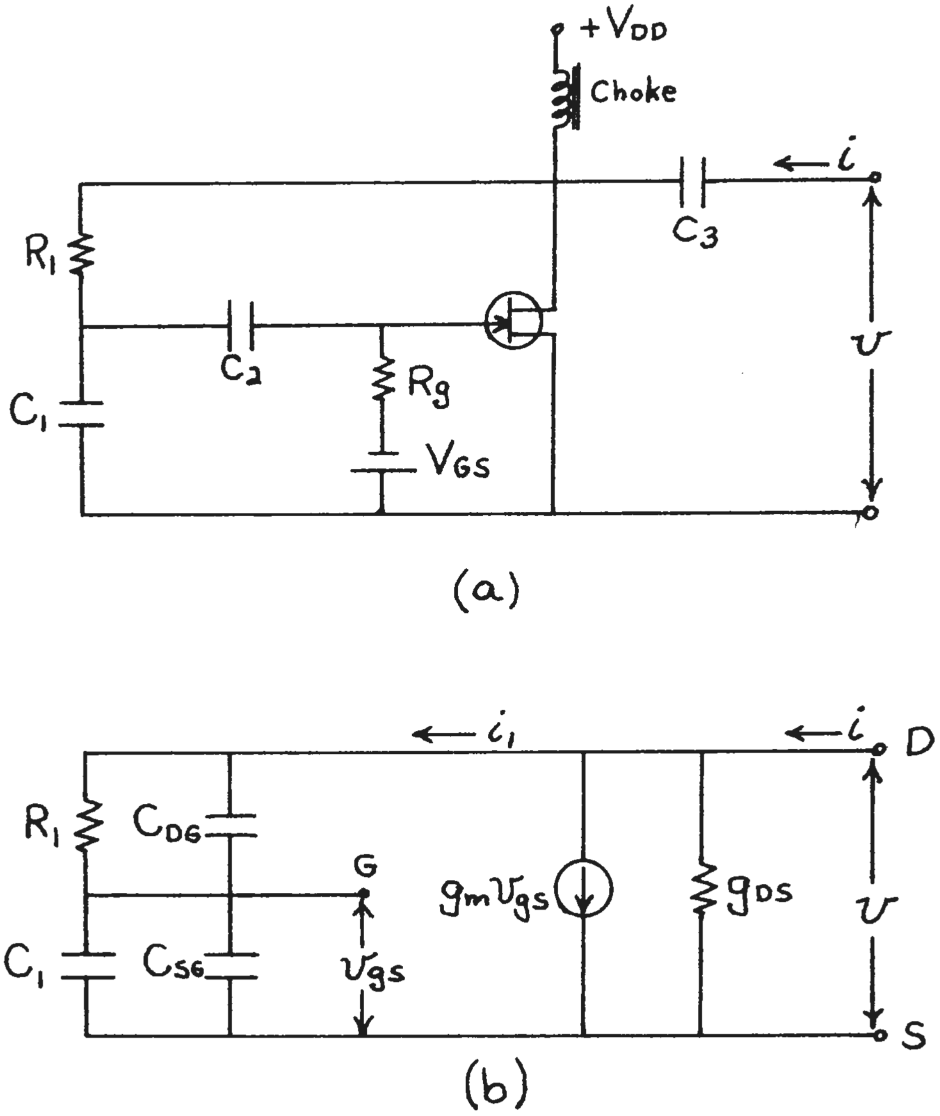


Figure 4. (a) Inductive reactance circuit employing an FET. (b) Dynamic equivalent circuit.

2. Approximate Analysis. For most field-effect transistors, C_{DG} and C_{SG} are small, with values of only a few pico-farads. As a first approach to the analysis of the circuit of Figure 4(b), assume R_1 is chosen so that at the frequency of interest,

$$R_1 \ll \frac{1}{\omega C_{DG}} \qquad (9)$$

Then neglecting C_{DG} and letting

$$C = C_1 + C_{SG} \qquad (10)$$

the equivalent circuit is simplified still further as shown in Figure 5.

When a voltage v is applied between drain and source, the current i that flows is given by

$$i = g_m v_{gs} + i_1 + g_{DS} v \qquad (11)$$

where i_1 is the current drawn by the feedback network. $g_{DS}v$ is a purely in-phase component of current and its only effect is to lower the effective Q. i_1 serves mainly to establish the gate voltage v_{gs}, and since it has a resistive component of current, it should be kept as small as possible. The current $g_m v_{gs}$ must be the dominant portion of the total current i. Since $g_m v_{gs}$ is to be inductive, and it has the same phase as v_{gs}, then v_{gs} should lag v by approximately 90 degrees.

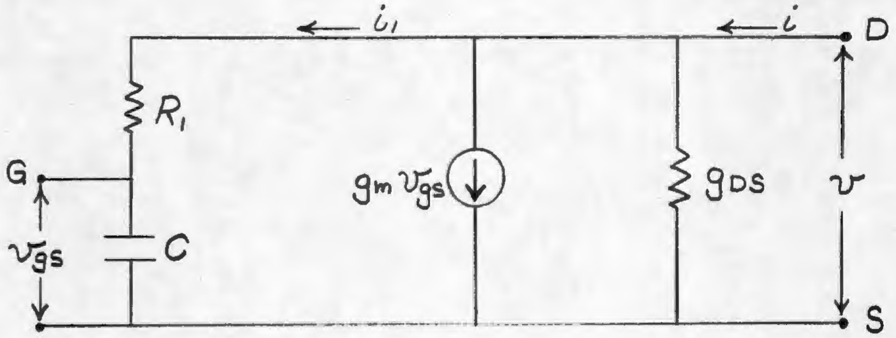


Figure 5. Approximate equivalent for the circuit of Figure 4(a).

These conditions can be realized if R_1 and C_1 are chosen so that

$$R_1 \gg \frac{1}{\omega C} \tag{12}$$

Then i_1 will be almost resistive, leading v by only a small phase angle. v_{gs} is the voltage across C produced by i_1, and will lag v by almost 90 degrees. These relationships are shown in the phasor diagram of Figure 6. The lengths and angles of the various vectors have been exaggerated for the sake of clarity.

Analytically,

$$i_1 = \frac{v}{R_1 - j\frac{1}{\omega C}} \tag{13}$$

$$v_{gs} = \frac{-j\frac{v}{\omega C}}{R_1 - j\frac{1}{\omega C}} \tag{14}$$

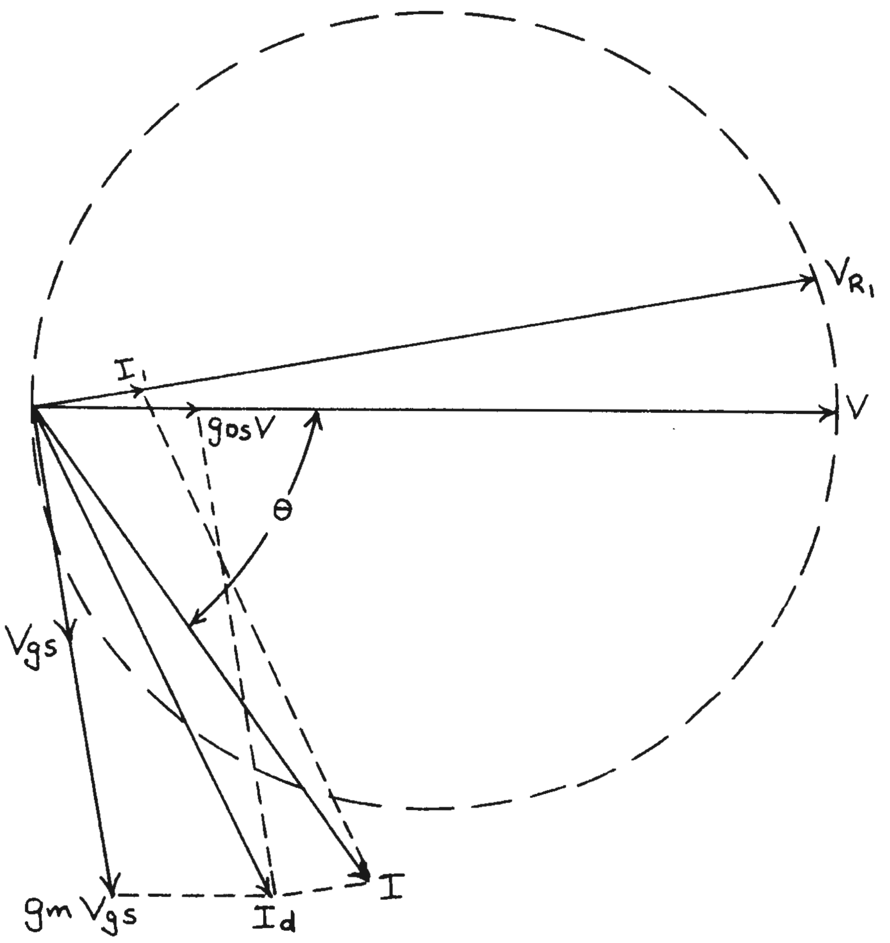


Figure 6. Phasor diagram showing voltage and current relationships in the simple inductive circuit of Figure 5.

Substituting these relationships into (11) yields

$$i = v \left[\frac{1 - j \frac{g_m}{\omega C}}{R_1 - j \frac{1}{\omega C}} + g_{DS} \right] \tag{15}$$

and the equivalent output admittance of the circuit is

$$Y_o = g_{DS} + \frac{1 - j \frac{g_m}{\omega C}}{R_1 - j \frac{1}{\omega C}} \tag{16}$$

When Y_o is separated into its real and imaginary parts, expressions for the equivalent conductance and susceptance are as follows:

$$G_o = g_{DS} + \frac{R_1 + \frac{g_m}{\omega^2 C^2}}{R_1^{\,2} + \frac{1}{\omega^2 C^2}} \tag{17}$$

$$B_o = \frac{1 - g_m R_1}{\omega C (R_1^{\,2} + \frac{1}{\omega^2 C^2})} \tag{18}$$

Applying the assumption of (12) to these expressions produces

$$G_o = g_{DS} + \frac{1}{R_1} \left(1 + \frac{g_m}{\omega^2 C^2 R_1}\right) \tag{19}$$

$$B_o = \frac{1}{\omega C R_1} \left(\frac{1}{R_1} - g_m \right) \tag{20}$$

Based on representative values of several milli-ohms for g_m, it is possible to have

$$R_1 \gg \frac{1}{g_m} \tag{21}$$

and still meet the other conditions on R_1 posed by (9) and (12). Therefore, the susceptance can be approximated by

$$B_o \approx -\frac{g_m}{\omega CR_1}. \tag{22}$$

Then, the approximate effective inductance and Q for the reactance circuit are

$$L_{eff} = \frac{-1}{\omega B_o} \approx \frac{CR_1}{g_m} \tag{23}$$

$$Q_{eff} = \frac{|B_o|}{G_o} \approx \frac{g_m}{\omega C \left(1 + g_{ds}R_1 + \frac{g_m}{\omega^2 C^2 R_1{}^2}\right)} \tag{24}$$

The accuracy of these approximate values depends, of course, on the validity of the assumptions (9), (12) and (21). g_m and C_{DG} will be fixed values for the device employed, while the product CR_1 is determined by the value of L_{eff} desired. At low frequencies it is probable that values of R_1 and C_1 can be chosen such that these approximated solutions are valid, and still obtain moderate values of effective inductance. At higher frequencies, R_1 and C_1 could be selected to satisfy (9) and (12), but the value of R_1 would be small and (21) would no longer be valid. Even though these solutions are not accurate at higher frequencies, they will still provide time-saving estimates for initial consideration in the design.

As mentioned previously, the circuit of Figure 4(a) can be changed into a capacitive reactance circuit by reversing the positions of R_1 and C_1. The resulting equivalent circuit is shown in Figure 7.

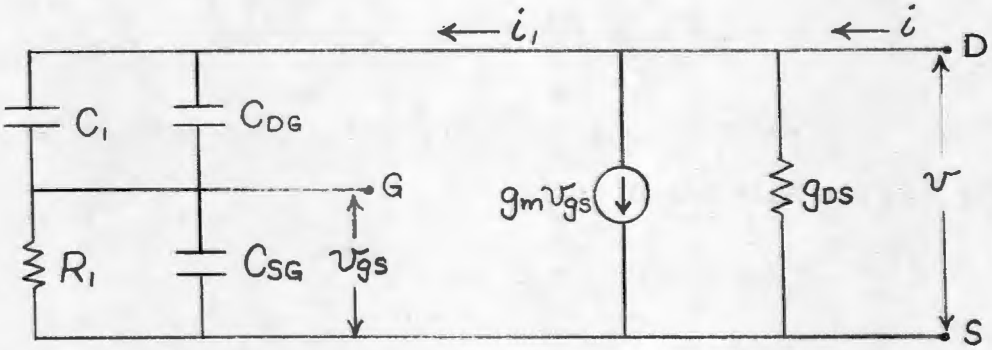


Figure 7. Dynamic equivalent for a simple capacitive reactance circuit.

An approximate analysis of this circuit can be carried out in the same manner as that used for the inductive circuit. Letting

$$C = C_1 + C_{DG} \tag{25}$$

and assuming

$$R_1 \ll \frac{1}{\omega C_{SG}} \tag{26}$$

C_{SG} can be neglected and the simplified equivalent circuit will be that shown in Figure 8(a). If R_1 and C_1 are chosen so that

$$R_1 \ll \frac{1}{\omega C} \tag{27}$$

then the voltage and current relationships in the circuit can be represented by the phasor diagram of Figure 8(b).

With the assumptions (26) and (27) taken into account, the approximate equivalent conductance and susceptance of the circuit are

$$G_o \approx g_{DS} + \omega^2 C^2 R_1 (g_m R_1 + 1) \tag{28}$$

$$B_o \approx \omega C (g_m R_1 + 1) \tag{29}$$

From these expressions, the effective capacitance and quality factor are found to be

$$C_{eff} \approx g_m C R_1 + C \tag{30}$$

$$Q_{eff} \approx \frac{\omega C (g_m R_1 + 1)}{g_{DS} + \omega^2 C^2 R_1 (g_m R_1 + 1)} \tag{31}$$

Again, these approximate solutions will give accurate estimates only when all of the assumptions are valid. With this capacitive reactance circuit however, it is possible to choose R_1 and C_1 so that these approximate solutions hold at much higher frequencies than they did for the inductive circuit considered previously. C_{DG} and C_{SG} will have approximately the same values, so if C_1 is sufficiently greater than C_{DG}, and R_1 is chosen to satisfy (27), then (26) will also be satisfied. Quite large values of C_{eff} can be achieved by making C_1 large, but R_1 must become smaller if (27) is to hold, and the voltage-variable range of the effective capacitance is reduced.

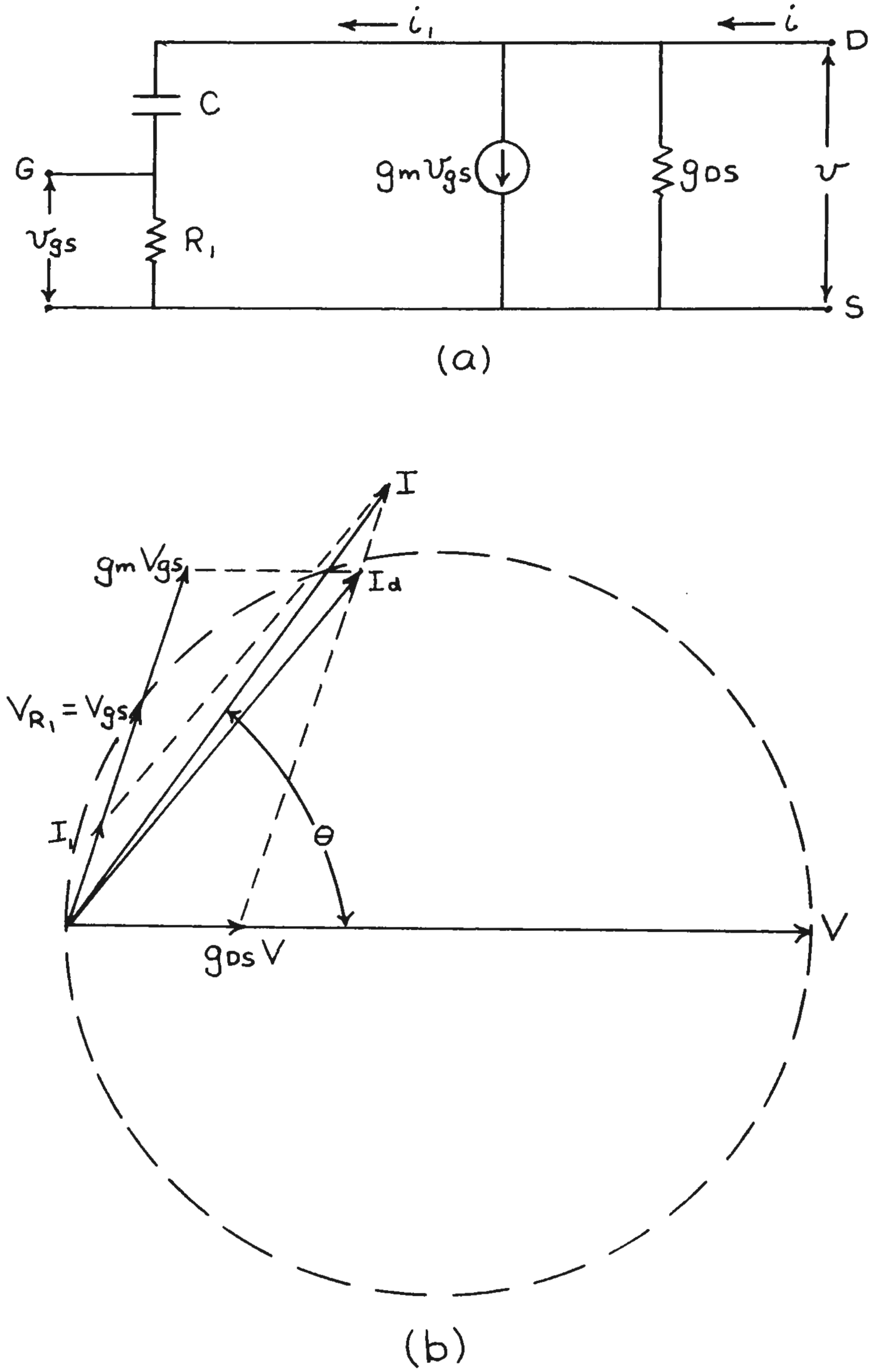


Figure 8. (a) Approximate form of the equivalent circuit shown in Figure 7. (b) Phasor diagram of voltage and current relationships in this circuit.

3. Exact Analysis. At frequencies of interest in this report, the assumptions made in the preceeding Section are not generally valid and exact solutions of the circuit models are required.

When the inductive circuit of Figure 4(b) is solved without simplification, the output admittance becomes

$$Y_o = g_{DS} + \frac{g_m Z_2 + 1}{Z_1 + Z_2} \qquad (32)$$

where

$$Z_1 = \frac{R_1 (- j \frac{1}{\omega C_{DG}})}{R_1 - j \frac{1}{\omega C_{DG}}} \qquad (33)$$

$$Z_2 = - j \frac{1}{\omega (C_1 + C_{SG}} \qquad (34)$$

Substituting (33) and (34) into (32), and separating the resulting expression into real and imaginary parts, yields

$$G_o = g_{DS} + \frac{g_m (1+R_1{}^2 \omega^2 C_{DG} C_T) + R_1 \omega^2 (C_1+C_{SG})^2}{1 = R_1{}^2 \omega^2 C_T{}^2} \qquad (35)$$

$$B_o = \frac{\omega (C_1+C_{SG})(1-g_m R_1+R_1{}^2 \omega^2 C_{DG} C_T)}{1 + R_1{}^2 \omega^2 C_T{}^2} \qquad (36)$$

where

$$C_T = C_1 + C_{SG} + C_{DG} \qquad (37)$$

The effective inductance and quality factor are then given by

$$L_{eff} = \frac{1+R_1^2\omega^2 C_T^2}{\omega^2(C_1+C_{SG})(1-g_m R_1+R_1^2\omega^2 C_{DG}C_T)} \tag{38}$$

$$Q_{eff} = \frac{\omega(C_1+C_{SG})(1-g_m R_1+R_1^2\omega^2 C_{DG}C_T)}{g_{DS}(1+R_1^2\omega^2 C_T^2) + g_m(1+R_1^2\omega^2 C_{DG}C_T) + R_1\omega^2(C_1+C_{SG})^2} \tag{39}$$

It can be verified that these expressions reduce to (23) and (24) respectively, when the appropriate assumptions are applied.

Although the junction capacitances will alter both the magnitude and Q of the equivalent inductance, only their effect on Q will be considered significant. With R_1 shunted by C_{DG}, the capacitive component of the feedback current i_1 is increased. Since v_{gs} still leads i_1 by 90 degrees, the total current i will lag v by a smaller phase angle than before, thus reducing Q_{eff}. C_{SG} must simply be combined with C_1 to obtain the total capacitance for that leg of the feedback network. To avoid unnecessary losses, it is still desirable to choose R_1 much greater than the reactance of C_1.

Turning now to the capacitive circuit of Figure 7, Y_o can again be expressed by (32), where

$$Z_1 = -j\frac{1}{\omega(C_1+C_{DG})} \tag{40}$$

$$Z_2 = \frac{R_1(-j\frac{1}{\omega C_{SG}})}{R_1 - j\frac{1}{\omega C_{SG}}} \tag{41}$$

Substituting these expressions into (32), and separating the result into its real and imaginary components produces rather lengthy expressions for the conductance and susceptance. These expressions are shortened by letting

$$X_1 = \frac{1}{\omega(C_1+C_{DG})} \tag{42}$$

$$X_2 = \frac{1}{\omega C_{SG}} \tag{43}$$

thus producing

$$G_o = g_{DS} + \frac{R_1X_2\left[(X_1+X_2)(g_mR_1+1) - X_1\right]}{X_1^2\,X_2^2 + R_1^2\,(X_1+X_2)^2} \tag{44}$$

$$B_o = \frac{R_1^2\,(X_1+X_2) + X_1^2\,X_2^2\,(g_mR_1+1)}{X_1^2\,X_2^2 + R_1^2\,(X_1+X_2)^2} \tag{45}$$

The effective capacitance and its quality factor are then given by

$$C_{eff} = \frac{R_1^2\,(X_1+X_2) + X_1X_2^2\,(g_mR_1+1)}{\omega\left[X_1^2\,X_2^2 + R_1^2\,(X_1+X_2)^2\right]} \tag{46}$$

$$Q_{eff} = \frac{R_1^2\,(X_1+X_2) + X_1X_2^2\,(g_mR_1+1)}{g_{DS}\left[X_1^2\,X_2^2 + R_1^2(X_1+X_2)^2\right] + R_1X_2\left[(X_1+X_2)(g_mR_1+1) - X_1\right]} \tag{47}$$

Although difficult to see in this form, these equations will reduce to the approximate relations of (30) and (31) respectively, if the appropriate assumptions are made.

If the reactance of the parallel combination of C_1 and C_{DG} is still much greater than R_1, then the feedback network current i_1 will still lead v by almost 90 degrees. However, with R_1 shunted by C_{SG}, v_{gs} will no longer be in phase with i_1, but will lag it by some small phase angle. Therefore the total current i will lead v by a lesser angle and Q_{eff} is again reduced.

It is seen then, from this exact analysis, that the junction capacitances serve only to reduce the quality of the reactance obtained, and to complicate the design problem. For this reason, field-effect transistors with small values of C_{DG} and C_{SG} should be selected when operating at higher frequencies.

4. Performance Characteristics. These first-order, R-C, phase-shift networks will produce a feedback voltage v_{gs} only in the first or the fourth quadrants, depending upon the order of R and C in the network. Consequently, the equivalent conductance cannot become negative, making these circuits inherently stable. Also, the phase and magnitude of the feedback voltage is not extremely sensitive to variations in component values. Combining these advantages with the simplicity of design makes these simple reactance circuits appear quite attractive.

Unfortunately, there are limitations in the performance of these circuits which seriously restrict their useful application. Referring to Figure 5, as the ratio of R_1

to the reactance of C′ is increased so that the phase angle between v and v_{gs} becomes more nearly 90 degrees, the magnitude of v_{gs} is reduced. Thus, high values of Q would be possible only for very small values of equivalent inductance. There is, however, the ever present current through g_{DS} which remains constant for a given operating point and applied voltage v. This in-phase current greatly reduces the values of Q attainable even at small values of equivalent inductance.

g_{DS} for most field-effect transistors is somewhat greater than $1/r_p$ for a pentode vacuum tube, while g_m is of the same order for both. Since only moderate Q values are obtained with similar circuits employing vacuum tubes, the Q values expected here will be even less. An equivalent argument arriving at the same conclusions can be carried out for the capacitive circuit of Figure 8(a). Therefore, it is seen that these simple reactance circuits, although capable of producing fairly large values of effective inductance or capacitance, will always exhibit low values of Q. Their applications are thus limited to circuits where this loss can be tolerated.

D. Reactance Circuits with Higher Q

1. General. To obtain higher Qs than these simple reactance circuits will afford, it is necessary to reduce or compensate for some of the losses. One method for doing this is to use a feedback network capable of producing a

voltage of sufficient magnitude which is truly 90 degrees out of phase with the applied voltage. This will overcome the limitation of the first-order R-C networks considered previously. However, there is still present the in-phase component of current through g_{DS}, and there will be some in-phase current drawn by the feedback network. These real positive currents could in effect be cancelled if $g_m v_{gs}$ was made to have a real negative component of current of equal magnitude. This is possible if the phase angle of v_{gs} is slightly greater than 90 degrees.

Although there are many circuits, both active and passive, which will produce phase shifts greater than 90 degrees, consideration will be given here to only one type of passive network.[6] The second-order R-C network shown in Figure 9(a) is capable of producing phase angles in the first and second quadrants, and represents a natural extension of the first-order network of Figure 5. The network of Figure 9(b) will produce phase angles in the third and fourth quadrants, and this represents an extension of the network shown in Figure 8(a). In both of these circuits, the actual phase angle and magnitude of the voltage v_1 are determined by the component values chosen. Since there is an infinite number of combinations of component values which will produce a given magnitude and phase of v_1, other factors must be considered.

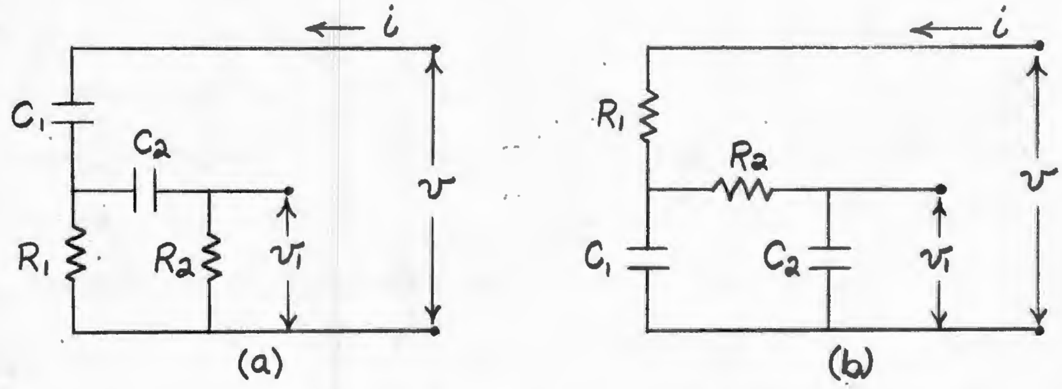


Figure 9. Second-order R-C phase shift networks.

First, the current i drawn by the feedback network should be small, not only to keep the in-phase component small and thus reduce the amount of compensating negative current required, but also to keep the reactive component small and thus maintain a broad range of voltage-variable control over the total reactance presented by the circuit. If i is to be small, then relatively large resistors and small capacitors should be employed.

A second factor concerns the ease with which calculations for design purposes can be carried out. Some pattern must be established which can be used to readily predict what effect changing component values will have on the magnitude and phase of v_1. A pattern will be established here by using a tapering parameter m to fix the relative values of the resistors and the capacitors in the network. If

$$R_1 = R \tag{48}$$

$$R_2 = mR \tag{49}$$

$$C_1 = C \tag{50}$$

and

$$C_2 = \frac{C}{m} \tag{51}$$

then v_1 will have a unique combination of magnitude and phase for each different set of R and C values. The networks of Figure 9 can then be solved for a large number of different values of R and C, and the results plotted to obtain curves in the complex plane of v_1 versus R for constant C, or v_1 versus C for constant R. From these curves the appropriate values of R and C can be selected to give v_1 with the desired magnitude and phase. It must be remembered that this set of curves will apply only for one value of the parameter m. If more than one value of m is to be considered, a separate set of curves for each value must be obtained.

The last, and perhaps the most important factor to be considered, is the sensitivity of the feedback voltage v_1 to component tolerances. In a reactance circuit, a small change in the phase of the feedback voltage can make the difference between obtaining a moderate-Q reactance, a high-Q reactance, or oscillations. Therefore, the stability and performance of the reactance circuit will depend greatly on the sensitivity of the phase-shift network.

There probably exist one or more combinations of component values out of all combinations which produce a given value of v_1, which will make v_1 least sensitive to component tolerances. No attempt will be made in this paper to find this optimum combination of values. However, if the design curves described in a preceeding paragraph are obtained for various values of m, they will indicate that some values of m produce a less sensitive value of v_1 than others. Thereby, at least some consideration of the sensitivity problem can be incorporated in the initial design.

When these feedback networks are used in conjunction with a field-effect transistor to obtain a reactance circuit, the junction capacitances of the device will become part of the total feedback network, and affect the voltage appearing at the gate. Whether or not these capacitances can be ignored depends upon the values of the network elements and the frequency of operation. Since it was stipulated earlier that relatively large resistances and small capacitances should be used to keep the current drawn by the feedback network small, and since the frequencies of interest are higher frequencies, then in general the junction capacitances cannot be ignored. In this case an approximate analysis would be almost useless; hence, these reactance circuits will be treated only in an exact form.

2. Capacitive Reactance Circuit. Figure 10(a) shows a capacitive reactance circuit employing the second-order, R-C, phase-shift network of Figure 9(a). Components C_3, C_4, R_g and the choke again serve only to properly bias the FET, and it is assumed that their values can be chosen so that they may be neglected at the frequency of operation. The equivalent dynamic model of this circuit will then be as

shown in Figure 10(b). As a design consideration, the tapering parameter m discussed previously will be applied to the R-C network so that resistors R_1 and R_2, and capacitors C_1 and C_2 will be related according to equations (48) through (52).

The total current drawn by the circuit will be given by (11), which is repeated here for convenience.

$$i = g_m v_{gs} + i_1 + g_{DS} v \tag{11}$$

The R-C network and the junction capacitances from a bridge circuit as redrawn in Figure 11, which must be solved to obtain v_{gs} and i_1. An unbalanced bridge of general impedances will be solved first, and then by substituting appropriate values, the solutions of the actual network will be obtained.

Loop currents and impedances to be used in the analysis are shown in the general bridge circuit of Figure 12. Applying Kirchhoff's voltage law around the three loops provides

$$\text{Loop 1:} \quad v = i_1(Z_1 + Z_4) + i_2 Z_1 + i_3 Z_4 \tag{52}$$

$$\text{Loop 2:} \quad 0 = i_1 Z_1 + i_2(Z_1 + Z_2 + Z_3) + i_3(-Z_3) \tag{53}$$

$$\text{Loop 3:} \quad 0 = i_1 Z_4 + i_2(-Z_3) + i_3(Z_3 + Z_4 + Z_5) \tag{54}$$

Solving this set of simultaneous equations for i_1 produces

$$i_1 = \frac{v}{D}\left[(Z_1 + Z_2 + Z_3)(Z_3 + Z_4 + Z_5) - Z_3^2\right] \tag{55}$$

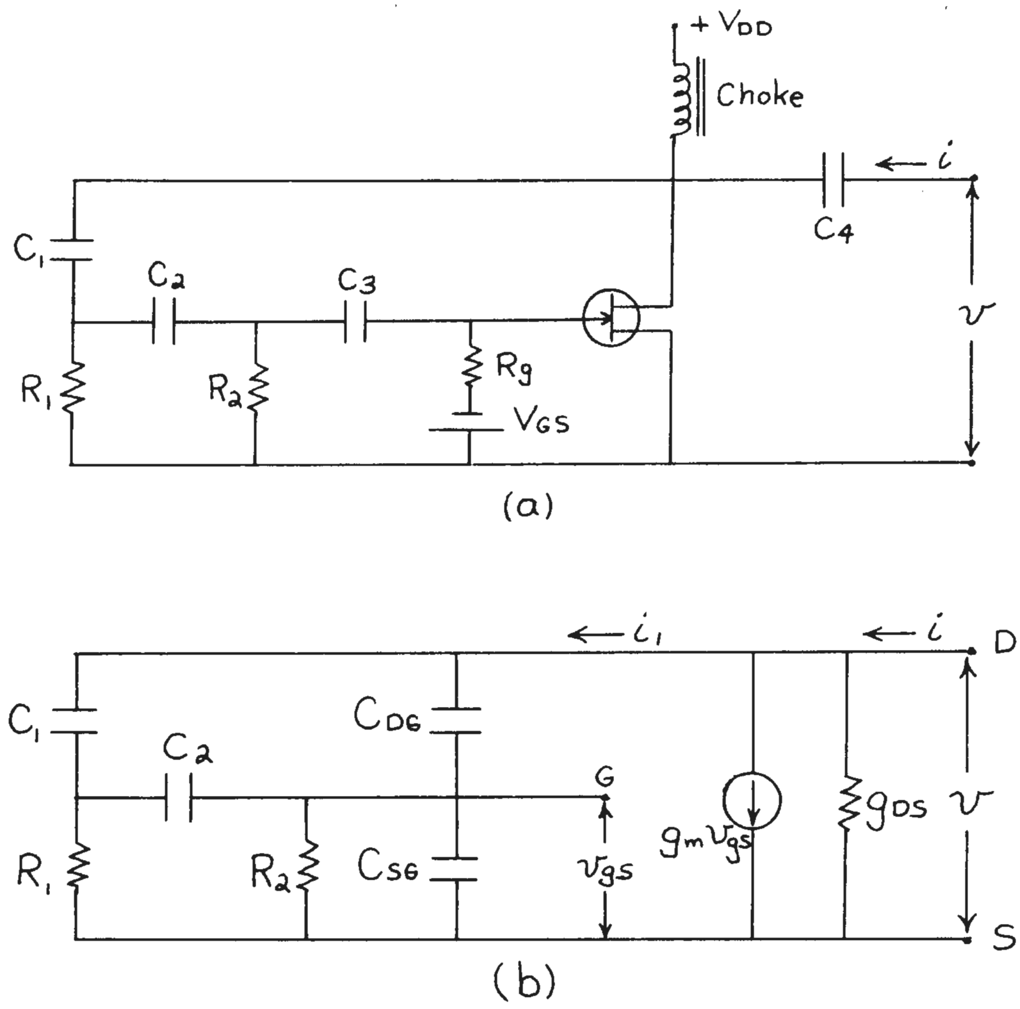


Figure 10. (a) Capacitive reactance circuit employing a second-order R-C feedback network. (b) Dynamic equivalent circuit.

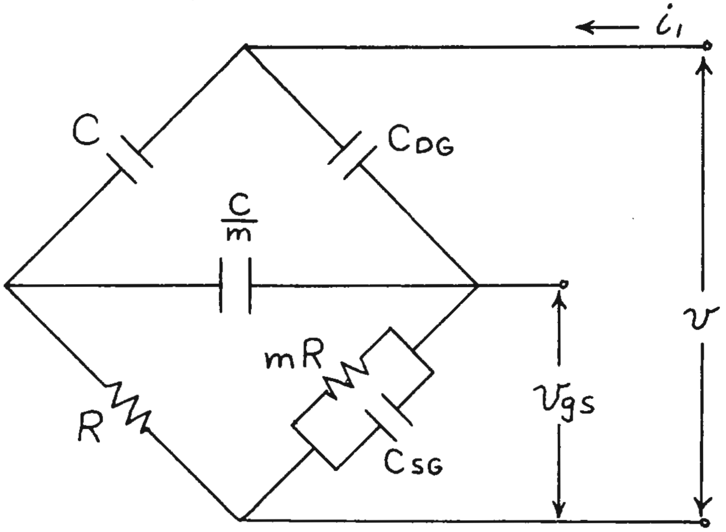


Figure 11. Bridge network in the circuit of Figure 10.

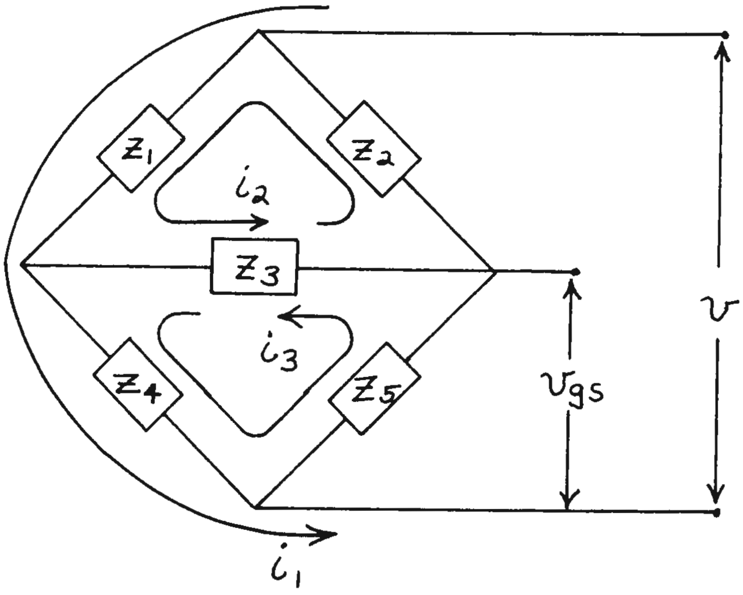


Figure 12. General impedance bridge showing loop currents used in the analysis.

where D is the determinant of coefficients given by

$$D = \begin{vmatrix} Z_1+Z_4 & Z_1 & Z_4 \\ Z_1 & Z_1+Z_2+Z_3 & -Z_3 \\ Z_4 & -Z_3 & Z_3+Z_4+Z_5 \end{vmatrix} \tag{56}$$

Now, since

$$v_{gs} = -i_3 Z_5 \tag{57}$$

solving for i_3 and substituting the resulting expression into (57) yields

$$v_{gs} = \frac{vZ_5}{D} \left[Z_1 Z_3 + Z_4(Z_1+Z_2+Z_3) \right] \tag{58}$$

These solutions for i_1 and v_{gs} will apply to the network of Figure 11, by letting

$$Z_1 = \frac{1}{j\omega C} \tag{59}$$

$$Z_2 = \frac{1}{j\omega C_{DG}} \tag{60}$$

$$Z_3 = \frac{m}{j\omega C} \tag{61}$$

$$Z_4 = R \tag{62}$$

$$Z_5 = \frac{\dfrac{mR}{j\omega C_{SG}}}{mR + \dfrac{1}{j\omega C_{SG}}} \tag{63}$$

The junction capacitances, C_{DG} and C_{SG}, may significantly affect the values of i_1 and v_{gs} obtained, and therefore their values must be known with some degree of accuracy, for the device employed.

As mentioned in the general discussion, the procedure here will be to solve equations (55) and (58) for a large number of R and C values, in order to obtain data for design purposes. Since the value of v will not affect the total reactance shown by the circuit as long as it is held within the operating range of the FET, it can be arbitrarily selected to have any value for design purposes.

Because of the great amount of labor and time required to carry out this analysis by hand, it is best accomplished with the aid of a digital computer. A simple program written in Fortran IV language for use with the IBM 360 Digital Computer is included in Appendix I. The applied voltage, the tapering parameter m, the values of the junction capacitances, and the frequency are entered as data. The program gives values of v_{gs} and i_1 over a range of R and C values, and draws curves of v_{gs} in the complex plane, for constant values of C and varying R.

The total admittance of the reactance circuit as obtained from (11) is

$$Y_o = \frac{g_m v_{gs}}{v} + \frac{i_1}{v} + g_{DS} \tag{64}$$

If v is selected to have a value of one, then the equivalent conductance and susceptance can be expressed by

$$G_o = g_{DS} + R_e(g_m v_{gs} + i_1) \tag{65}$$

$$B_o = I_m(g_m v_{gs} + i_1) \tag{66}$$

and these real and imaginary components will be directly available from the design data. Writing this in terms of the effective capacitance and Q yields

$$C_{eff} = \frac{1}{\omega} I_m(g_m v_{gs} + i_1) \tag{67}$$

$$Q_{eff} = \frac{I_m(g_m v_{gs} + i_1)}{g_{DS} + R_e(g_m v_{gs} + i_1)} \tag{68}$$

It is desirable to make G_o as small as possible to obtain high Q, but it must never be allowed to go negative or oscillations will result. By letting the $R_e(v_{gs} + i_1)$ go negative, it subtracts from the positive conductance of g_{DS}, and higher values of Q are obtained. The stability limit that must not be exceeded is

$$R_e(g_m v_{gs} + i_1) \geq -g_{DS} \tag{69}$$

It must be pointed out that when this capacitive reactance circuit is used in conjunction with a real inductor which has a finite conductance g_L, the stability limit becomes

$$R_e(g_m v_{gs} + i_1) \geq -(g_{DS} + g_L) \tag{70}$$

The negative conductance of the reactance circuit can thus provide Q multiplication^8 in the circuit where it is employed.

For a given value of the tapering parameter m, it may not be possible to select values of R and C which will provide specified values of both C_{eff} and Q_{eff}. Without going to a different value of m, a compromise can be made depending upon which property is the most important in the particular application. Usually most of the device characteristics are not known with sufficient accuracy to warrant too exact an analysis.

It must also be remembered that the values of g_m, g_{DS}, and the junction capacitances are all bias dependent. This must be taken into account especially from a stability standpoint. If gate bias is to be used to vary g_m, and thus the effective capacitance shown by the circuit, then the circuit must be stable at each and every bias level. This means that equation (69) must be satisfied over the entire bias range.

3. Inductive Reactance Circuit. An inductive reactance circuit employing the second order R-C network of Figure 9(b), is shown along with its dynamic equivalent in Figure 13. The R-C network and the junction capacitances of the FET again form a bridge circuit at the gate, which is redrawn in Figure 14. The tapering parameter m has been included to fix the relative values in the network. The solutions obtained for the general impedance bridge of Figure 12 can be applied here in the same manner as they were in the capacitive reactance circuit by letting

$$Z_1 = R \tag{71}$$

$$Z_2 = \frac{1}{j\omega C_{DG}} \tag{72}$$

$$Z_3 = mR \tag{73}$$

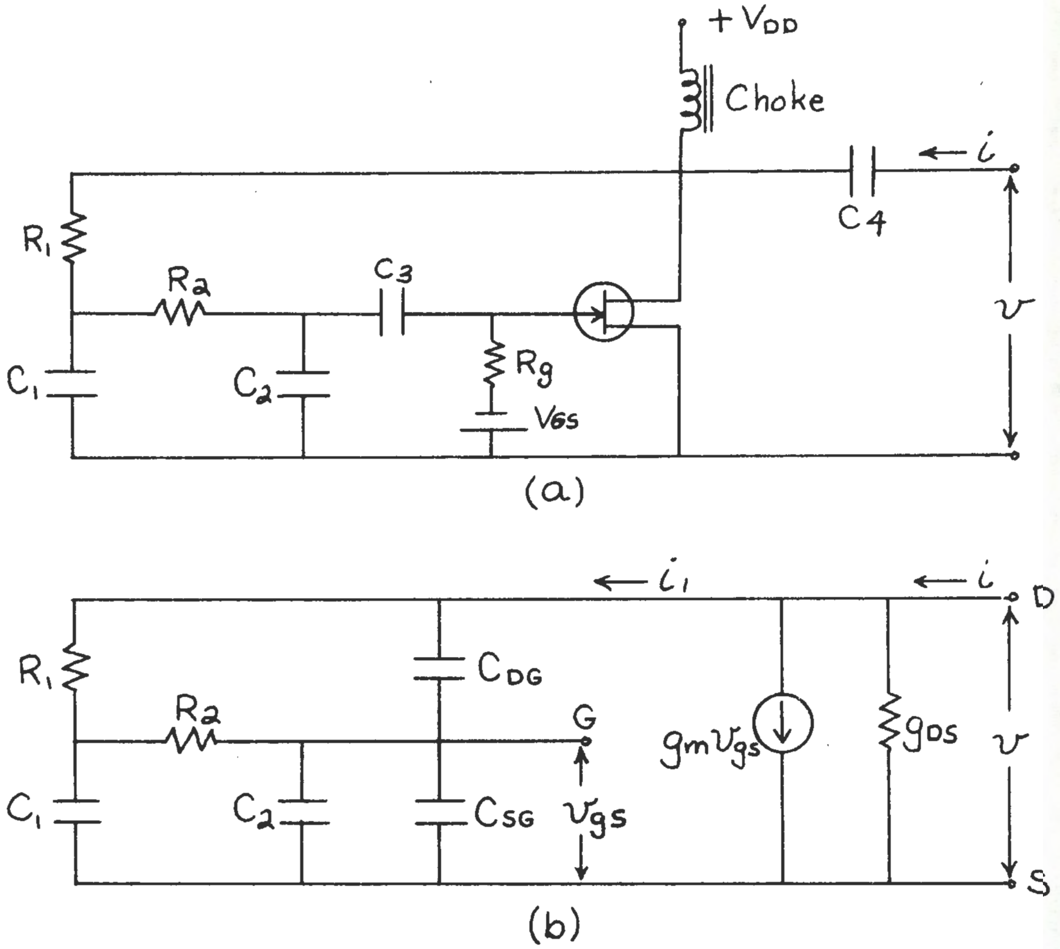


Figure 13. (a) Inductive reactance circuit employing a second-order R-C feedback network. (b) Dynamic equivalent circuit.

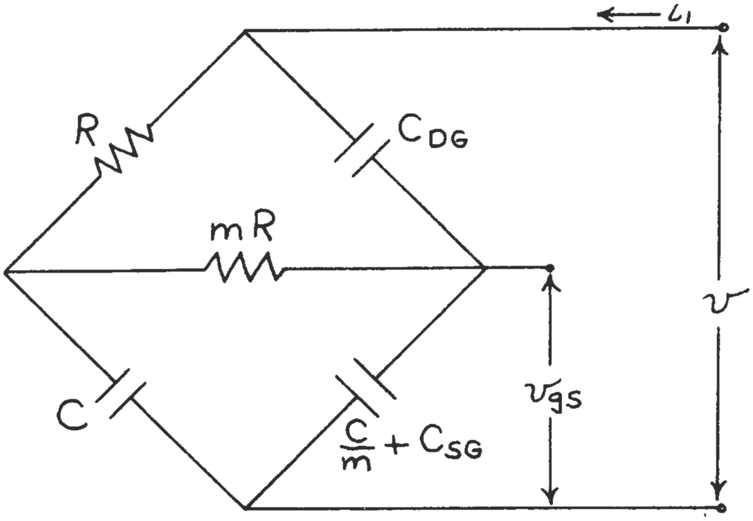


Figure 14. Bridge network in the circuit of Figure 13.

$$Z_4 = \frac{1}{j\omega C} \tag{74}$$

$$Z_5 = \frac{m}{j\omega(C + mC_{SG})} \tag{75}$$

Then i_1 and v_{gs} are given by (55) and (58) respectively. With slight modificationsto allow for the component changes, the computer program in Appendix I can also be used to obtain design data and curves for this inductive circuit.

Carrying out an analysis similar to the previous one, the effective inductance and Q are found to be

$$L_{eff} = \frac{-1}{\omega\ I_m(g_m v_{gs} + i_1)} \tag{76}$$

$$Q_{eff} = \frac{I_m(g_m v_{gs} + i_1)}{g_{DS} + R_e(g_m v_{gs} + i_1)} \tag{77}$$

Statements made about the capacitive circuit concerning stability also apply here. It must be cautioned, however, that if this inductive reactance circuit is not used in conjunction with another inductor, the stability limit of equation (69) must be definitely avoided.

No attempt has been made in any of these circuit designs to allow for stray capacitance or inductive coupling. Excessive or even small amounts of either of these may upset the design and they should therefore be given serious consideration when fabricating an actual circuit.

III. EXPERIMENTAL RESULTS

A. Measuring Technique

1. Q-Meter. Prior to the actual fabrication of a reactance circuit, a method for measuring its properties had to be selected. The frequencies of interest were in the 200-250 Khz range, where a possibility exists for employing these reactance circuits in teletype applications. A standard Q-meter appeared to be the simplest and most direct means of measuring an equivalent dynamic inductance or capacitance and its associated quality factor. The instrument selected was a Boonton Q-Meter type 260-A, which offered operating frequencies in the range of interest.

The measuring principle of this instrument is based on a familiar characteristic of series-resonant circuits; namely, that the magnitude of the voltage appearing across either reactor is equal to the voltage applied to the circuit multiplied by the circuit Q.[9] Referring to Figure 15, the voltage is applied across a 0.02-ohm resistor, and a calibrated, internal, vacuum-tube voltmeter is used to measure the voltage appearing across one of the reactances. C_Q is an internal capacitor of the Q-meter which is varied to establish resonance in the measuring circuit. Its dial is calibrated to read capacitance, but will also give direct readings of inductance at certain frequencies. One of these frequencies is 250 Khz, and to take advantage of any simplification which might result in the measuring process, this frequency was used for all of the reactance circuit measurements.

Three basic methods, direct, parallel, and series, exist for connecting components to the Q-meter measuring circuit. Only the first two of these methods will be considered, since the series connection was not required in any of the measurements.

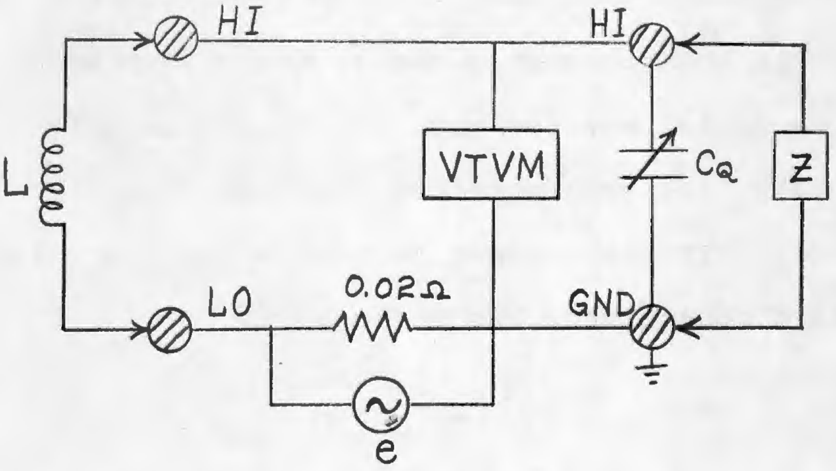


Figure 15. Q-meter parallel measuring circuit.

At 250 Khz, direct measurement of inductors with values from 1 to 10mh is possible. The unknown inductance is connected across the HI-LO terminals of the Q-meter, and the other terminals are left open. After the circuit is brought to resonance by varying C_Q, the value of the inductance can be read directly from the tuning capacitor dial. The value of Q indicated on the Q meter is the circuit Q, but since the tuning capacitor is essentially lossless, this value will be the Q of the inductance.

A parallel connection can be used to measure capacitances of less than 430 pf, and certain small inductances.

A standard work coil is required which will resonate with the tuning capacitor at the selected frequency. First, the standard coil is connected directly across the HI-LO terminals and with the other terminals open, the circuit is brought to resonance. The Q reading and the value of C_Q are recorded as Q_1 and C_1 respectively. The unknown reactance is then connected across the HI-GND terminals, and resonance is restored with the tuning capacitor. Values of C_2 and Q_2 are then obtained from the capacitor dial and the Q meter. If the unknown reactance is capacitive, its effective capacitance and Q are given by

$$C_{eff} = C_1 - C_2 \tag{78}$$

$$Q_{eff} = \frac{Q_1 Q_2 (C_1 - C_2)}{\Delta Q C_1} \tag{79}$$

where

$$\Delta Q = Q_1 - Q_2 \tag{80}$$

If the unknown reactance is inductive, then its effective inductance and Q are given by

$$L_{eff} = \frac{1}{\omega^2 (C_2 - C_1)} \tag{81}$$

$$Q_{eff} = \frac{Q_1 Q_2 (C_2 - C_1)}{\Delta Q C_1} \tag{82}$$

2. Varactor Measurements. To test this measuring technique, it was decided to measure the capacitance and Q of several voltage-variable capacitance diodes, known as varactors. These semiconductor devices operate on the prin-

ciple that the depletion layer of the p-n junction widens with reverse bias. This in effect moves the two conduction areas apart and decreases the junction capacitance. Specially designed varactors are available with capacitance values up to several thousand picofarads, but unfortunately they are quite expensive. By contrast, the varactors used here have maximum values of 100 pf and are relatively inexpensive. Varactors are widely used in some of the same applications where capacitive reactance circuits could be employed, and thus it is worthwhile to note their characteristics for future reference.

The simple circuit arrangement shown in Figure 16 was used in the varactor measurements. V_{RR} is a variable voltage supply used to reverse bias the varactor. The 0.5-μf capacitor, which offers negligible reactance at the measuring frequency, serves to block the d.c. voltage from entering the Q-meter. The 2-Megohm resistor offers a high-impedance path through the bias supply and thus prevents an a.c. short across the varactor. Since the measuring method to be used is the parallel connection, equations (78) and (79) apply, and a standard coil was selected with a value of 2.5 mh and a Q of approximately 180.

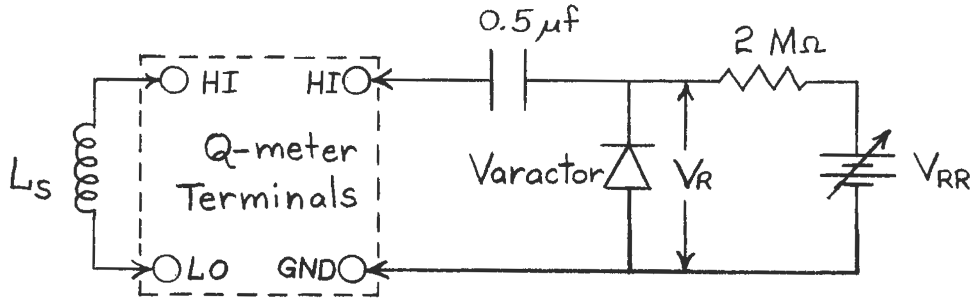


Figure 16. Varactor measuring circuit.

The equivalent circuit of the reactance measured between the HI-GND terminals is shown in Figure 17, if the entire circuit is removed in the measuring process. It would be more realistic to measure the properties of a varactor in this manner, because an associated bias circuit is always required. However, it is desired here to obtain values of C_V and Q_V for comparison with the manufacturer's specifications and thus prove or disprove the validity of this measuring technique.

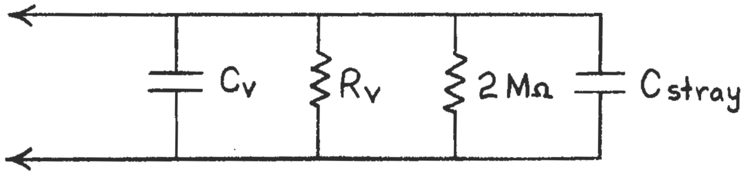


Figure 17. Equivalent circuit of the varactor and its biasing network.

If the circuit remains connected during the measuring process, and only the varactor is removed, an accurate value of C_V will be obtained. The measured value of Q_V will be correct only if $R_V \ll 2$ MΩ, but at 250 Khz, R_V will generally be much greater than 2 Megohms. The value of Q_V, although in reality very high, will then appear almost infinite. To study this effect, an ordinary capacitor with a directly measured capacitance of 97.4 pf and Q of 2105, was inserted in place of the varactor in the measuring circuit. The values of capacitance and Q then measured were 97.7 pf and 1970 respectively. Thus, it is seen that at least up to this value of Q, the 2-Megohm resistor does not produce any great inaccuracy. Since components with Qs higher than this usually introduce negligible losses in circuits where they appear, the actual value becomes insignificant and the procedure employed here appears to be adequate.

The varactors obtained for testing were Motorola types MV 840, MV 1650, and MV 1750. All were listed as having a capacitance of 100 pf at V_R = -4 volts, and a maximum to minimum capacitance ratio of approximately 2.5. The maximum reverse breakdown voltage was given as -30 volts for the MV 840 and MV 1750, and -20 volts for the MV 1650. Values of Q_V were given only at 50 Mhz which is just outside the usable frequency range of the Q-meter. The MV 840, being the least expensive and having by far the highest losses of the three, is reported to have a Q of 15 at this frequency.

With the test circuit in place, minus the varactor, values of C_1 and Q_1 to be used in equations (78) and (79), were found to be 153.6 pf and 127 respectively. The varactor was then inserted, and values of C_2 and Q_2 were obtained at different bias levels of V_R over its allowed range. Values of C_2 and the computed C_v for each varactor and bias level are listed in Table I. In all cases Q_2 was approximately the same as Q_1, indicating a very high Q_v at this frequency. For this reason, values of Q_2 and Q_v have not been listed in the table.

From the data in Table I, curves of C_v versus V_R, as shown in Figure 18, were obtained for the three different varactors. The curves for the MV 840 and the MV 1750 were almost coincident, and the curve drawn is representative of the capacitance for both.

To establish some validity for the Q measuring technique, it was decided to use a fixed bias level on the MV 840, and measure its capacitance and Q as a function of frequency. V_R was selected to be -30 volts, and the data obtained, along with the computed values of C_V and Q_V using (78) and (79), are listed in Table II. 44 Mhz was the highest frequency at which resonance could be obtained using a 0.1-μh standard coil, which was the smallest available. Curves of C_v and Q_v versus frequency, constructed from this data, are shown in Figure 19. From the Q_v value of 18 at 44 Mhz and the general shape of the curve, the projected value at 50 Mhz would approximate the manufacturer's listed value of 15.

The generally close agreement between the listed values and those measured by this method shows that this measuring technique should be satisfactory for measuring

TABLE I

Tabulated data and results from varactor capacitance measurements. C_1 = 153.6 pf, Q_1 = 127 for all cases.

	MV 840		MV 1650		MV 1750	
VR (volts)	C_2 (pf)	C_v (pf)	C_2 (pf)	C_v (pf)	C_2 (pf)	C_v (pf)
-30.0	112.9	40.7			112.2	41.4
-28.0	111.6	42.0			111.0	42.6
-26.0	110.2	43.4			109.4	44.2
-24.0	108.5	45.1			107.7	45.9
-22.0	106.7	46.9			105.8	47.8
-20.0	104.7	48.9	112.0	41.6	103.6	50.0
-19.0	103.6	50.0	110.4	43.2	102.4	51.2
-18.0	102.3	51.3	108.5	45.1	101.2	52.4
-17.0	101.0	52.6	106.5	47.1	99.7	53.9
-16.0	99.6	54.0	104.5	49.1	98.3	55.3
-15.0	97.8	55.8	102.4	51.2	96.6	57.0
-14.0	95.9	57.7	100.0	53.6	94.6	59.0
-13.0	94.0	59.6	97.7	55.9	92.7	60.9
-12.0	91.9	61.7	94.5	59.1	90.5	63.1
-11.0	89.4	64.2	92.0	61.6	88.2	65.4
-10.0	86.8	66.8	88.7	64.9	85.7	67.9
-9.5	85.2	68.4	87.0	66.6	84.2	69.4
-9.0	83.7	69.9	85.2	68.4	82.6	71.0
-8.5	81.9	71.7	83.2	70.4	80.7	72.9
-8.0	79.9	73.7	81.0	72.6	78.7	74.9
-7.5	77.8	75.8	78.7	74.9	76.5	77.1
-7.0	75.4	78.2	76.0	77.6	74.3	79.3
-6.5	72.8	80.8	73.3	80.3	71.9	81.7
-6.0	70.0	83.6	70.5	83.1	69.2	84.4
-5.5	66.9	86.7	67.0	86.6	66.0	87.6
-5.0	63.0	90.6	63.3	90.3	62.4	91.2
-4.5	59.0	94.6	58.9	94.7	58.7	94.9
-4.0	54.1	99.5	53.7	99.9	53.3	100.3

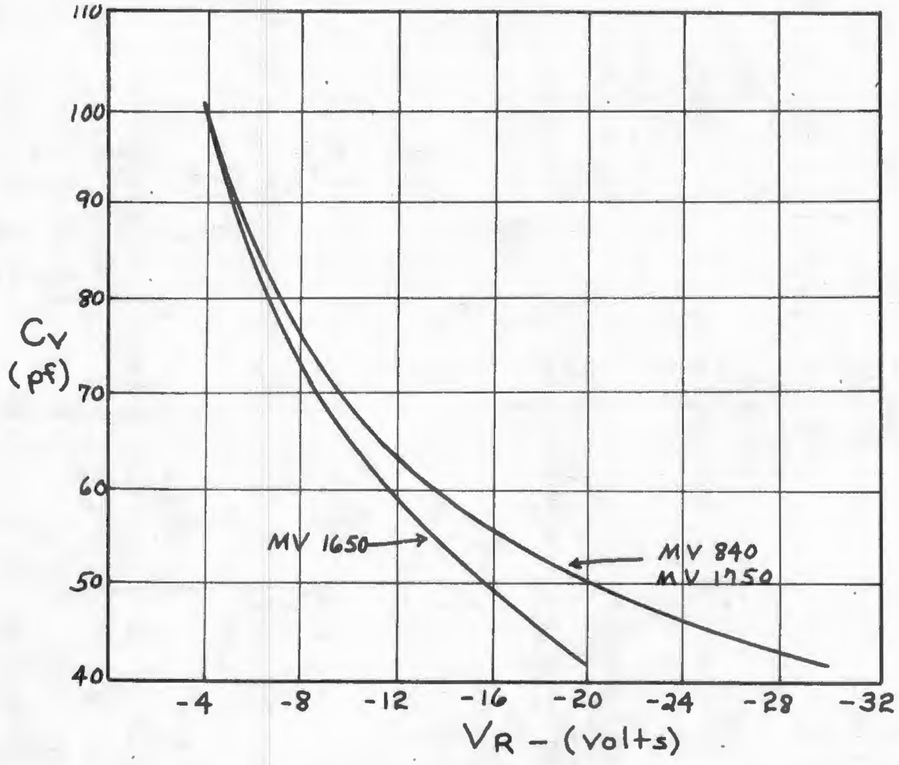


Figure 18. Varactor capacitors variation with reverse bias.

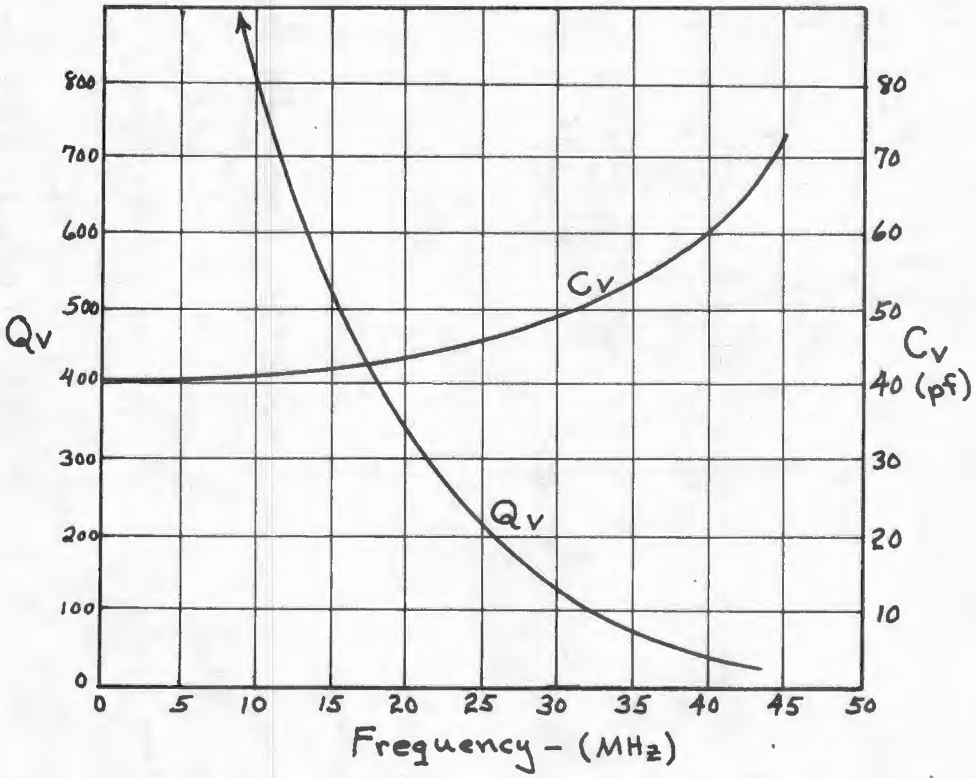


Figure 19. Variation of capacitance and Q with frequency for the MV 840 Varactor at $V_R = -30$ volts.

TABLE II

MV 840 Varactor capacitance and Q obtained for various frequencies with $V_R = -30$ volts.

f (Mhz)	Q_1	C_1 (pf)	Q_2	C_2 (pf)	C_v (pf)	Q_v
.25	127	153.6	127	112.9	40.7	
1	168	92.5	167	51.8	40.7	12,350
5	198	90.7	188	49.8	40.9	1680
10	188	238.0	181	196.6	41.4	803
22	113	433.6	108	391.5	42.1	237
25	113	335.8	106	291.7	44.1	209
30	138	231.3	115	184.0	47.3	141
33	144	190.5	106	140.7	49.8	105
37	149	151.3	70	95.1	56.2	49
40	152	128.7	44	67.5	62.2	30
44	155	105.0	23	34.7	70.3	18

the effective capacitance and Q of a reactance circuit. There is no apparent reason why equal success should not be possible when measuring inductive reactance circuits.

B. Model Verification Using a Simple Capacitive Reactance Circuit

The next step in the investigation appeared to be the construction of a simple capacitive reactance circuit. Although it was realized that such a circuit is limited in application by its low Q, general agreement of its properties with the theory of Chapter II would provide experimental verification of the FET model.

A reactance circuit employing a 2N3819 FET was fabricated according to the schematic diagram shown in Figure 20. This device was selected for its availability as well

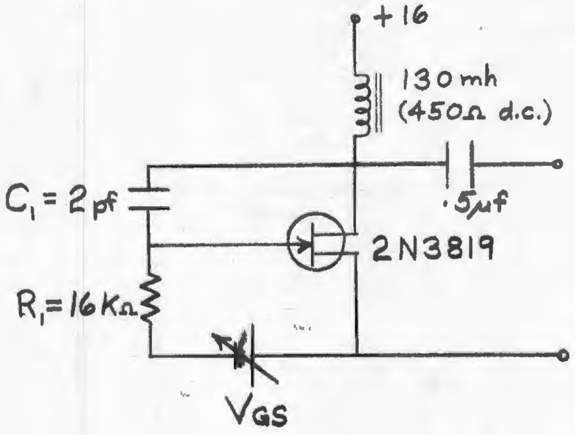
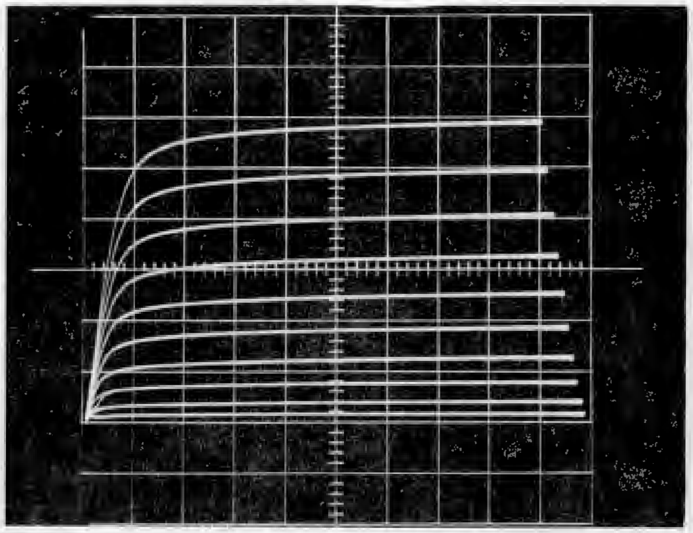


Figure 20. Simple capacitive reactance circuit.

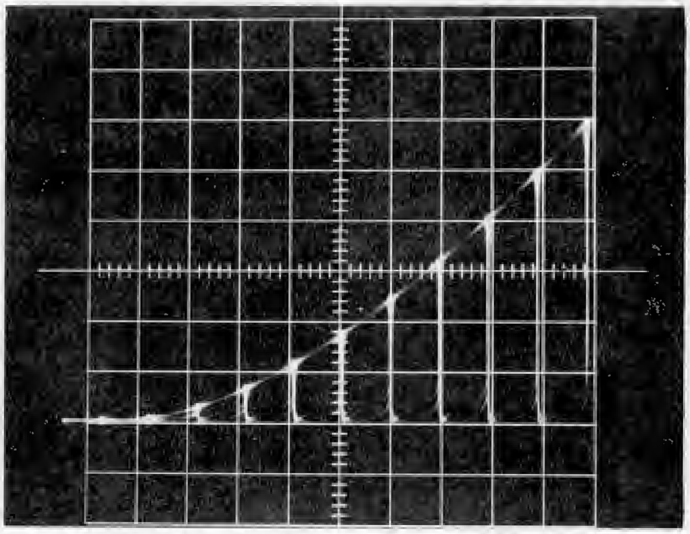
as its properties, and may not be the best FET that could be employed. It does however, offer high transconductance, relatively low output admittance, and small values of junction capacitances, which are all desirable properties for this application.

The common source drain and transfer characteristics for the particular 2N3819 employed, as obtained from the Tektronix type 575 Transistor Curve Tracer, are shown in Figure 21. With the static load line determined by only the 450 ohm d.c. resistance of the inductor, a drain supply of 16 volts was thought to be adequate. Although the transfer characteristic curve was obtained for V_{DD} = 20 volts, there was essentially no change in the observed curve in going to 16 volts.

Values of g_{DS} and g_m were obtained by measuring the slopes of the drain and transfer characteristic curves at



(a) Common-source drain characteristics for the 2N3819. Horizontal scale for V_{DS} 2 volts/div. Vertical scale for I_D is 1 ma/div. Top curve corresponds to $V_{GS}=0$, with steps of -.2 volts/step.



(b) Common-source transfer characteristic for the 2N3819 with V_{DS} =20 volts. Horizontal scale for V_{GS} is -.2 volts/div with V_{GS} = 0 at the right hand limit. Vertical scale for I_D is 1 ma/div.

Figure 21.

various values of V_{GS} along the load line. Admittedly, the individual values obtained by this method can be quite inaccurate, but by plotting the values and then passing a smooth curve through these points, reasonably accurate descriptions of these parameters should result. This was done to obtain the smooth curves shown in Figure 22. The variation of g_{DS}, through probably not linear in reality, was best represented by a linear curve over most of its range. Fixed gate bias was used in the circuit of Figure 20, so that its value could be easily controlled.

The equivalent circuit will be that shown in Figure 7, with one exception. The choke is of such a value that it cannot be neglected at 250 Khz. Since it appears between the drain and source, its inductive susceptance subtracts from the total capacitive susceptance and thus reduces the effective capacitance shown by the circuit. This effect is relatively small, amounting to a reduction in capacitance of only 3.2 pf. A more serious result is the reduction in Q caused by the additional losses that are introduced.

The junction capacitances were not known exactly, but based on the listed maximum values of C_{iss} and C_{rss} (8 pf and 4 pf respectively), the values of C_{DG} and C_{SG} should be no greater than 4 pf. With this knowledge, the values of R_1 and C_1 were selected so that the approximate solutions given by (30) and (31) would apply. Using values of g_{DS} and g_m for $V_{GS} = -1.0$ volts, and 4 pf each for C_{DG} and C_{SG},

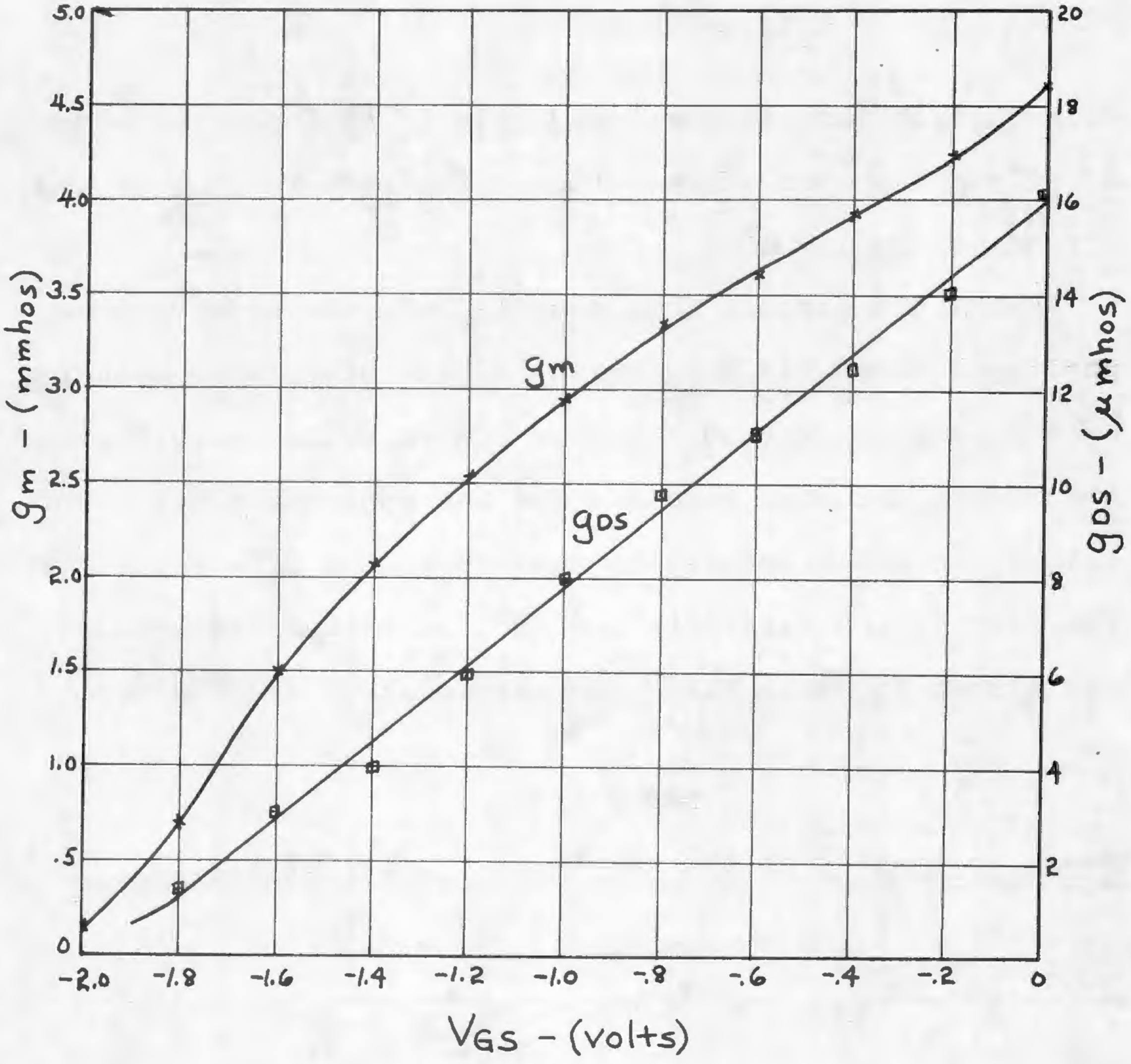


Figure 22. g_m and g_{DS} versus V_{GS} for the 2N3819 employed.

these equations yield the following expected values of C_{eff} and Q_{eff} for the circuit.

$$C_{eff} \approx 290 \text{ pf}$$

$$Q_{eff} \approx 5.9$$

This calculation was performed only to indicate the order of values expected and no attempt was made to include the effect of the inductor.

With the circuit thus established, the effective capacitance and Q, as a function of gate bias, were measured by the parallel method. Unlike the varactor measurements, the values obtained here are for the entire circuit. For all of the measurements, C_1 was 398 pf and Q_1 was 177. The rest of the data obtained and the calculated results are listed in Table III. The rather large discrepancy

TABLE III

Measured results of the reactance circuit of Fig.20.

V_{GS} (volts)	V_{DS} (volts)	Q_2	C_2 (pf)	C_{eff} (pf)	Q_{eff}
0	13.8	3.0	138	260	2.00
-.2	14.0	3.5	152	246	2.20
-.4	14.4	4.0	168	230	2.36
-.6	14.7	4.5	183	215	2.50
-.8	15.0	5.0	198	200	2.80
-1.0	15.2	7.0	217	181	3.32
-1.2	15.5	9.0	240	158	3.77
-1.4	15.7	11.0	265	133	3.92
-1.6	15.8	14.5	294	104	4.13
-1.8	15.9	22.5	330	68	4.41
-2.0	15.9	60.0	372	26	5.93
-2.2	16.0	110.0	382	16	11.70

between the calculated and measured values of C_{eff} at $V_{GS} = -1.0$ volts indicated that C_{DG} was actually smaller than the value assumed. By removing the external capacitor and thus using only C_{DG} as the feedback capacitance, it was hoped that an indication of the actual value could be obtained. The measured data and calculated results for this modified circuit are listed in Table IV.

For comparison to these measured values, a simple computer program (Appendix II) was written to evaluate the exact expressions, (46) and (47), which were appropriately modified to account for the effects of the inductor. Solutions were obtained over the range of V_{GS} for C having values of 2, 3, and 4 picofarads, where $C = C_1 + C_{DG}$. The effect of C_{SG} is small, and was chosen to be 4 pf as a worst case. The values of g_{DS} and g_m used were those taken

TABLE IV

Measured results of the modified reactance circuit with $C_1 = 0$.

V_{GS} (volts)	V_{DS} (volts)	Q_2	C_2 (pf)	C_{eff} (pf)	Q_{eff}
0	13.8	10.5	263	135	3.79
-.2	14.0	11.2	272	126	3.79
-.4	14.4	12.2	280	118	3.89
-.6	14.7	13.2	287	111	3.98
-.8	15.0	15.0	296	102	4.22
-1.0	15.2	16.7	303	95	4.39
-1.2	15.5	19.2	315	83	4.49
-1.4	15.7	23.0	327	71	4.72
-1.6	15.8	29.5	341	57	5.07
-1.8	15.9	45.0	361	37	5.61
-2.0	15.9	96.0	382	16	8.44
-2.2	16.0	152.0	390	8	21.65

from the curves of Figure 22.

These calculated values of C_{eff} have been plotted in Figure 23, along with the measured values listed in Tables III and IV. The general agreement between the calculated values when C = 2 pf and the measured values when $C = C_{DG}$, would indicate that the value of C_{DG} is very close to 2 pf, providing that the model used in the analysis was correct. The general agreement between the calculated values when C = 4 pf and the measured values when $C = C_{DG} + 2$ pf, not only supports a value of 2 pf for C_{DG}, but also tends to verify the model employed.

The agreement between measured and calculated values of Q_{eff} is not quite as good, as seen by Figure 24. The lower values of measured Q at higher currents, could be attributed to current-dependent losses in the circuit, not accounted for in the model. The sharp rise in measured Q at large values of gate bias, results when pinch-off is approached. When these extremes are avoided, the calculated and measured values of Q_{eff} differ nowhere by more than a factor of 2, which can be considered adequate in the design of these circuits.

The results obtained here show that the circuit model chosen provides an adequate description of the simple reactance circuit, especially in the range of V_{GS} from -.4 to -1.6 volts. As expected, the effective Q of this circuit was quite low, but the additional knowledge of the FET model obtained should facilitate the design of reactance circuits with higher Q.

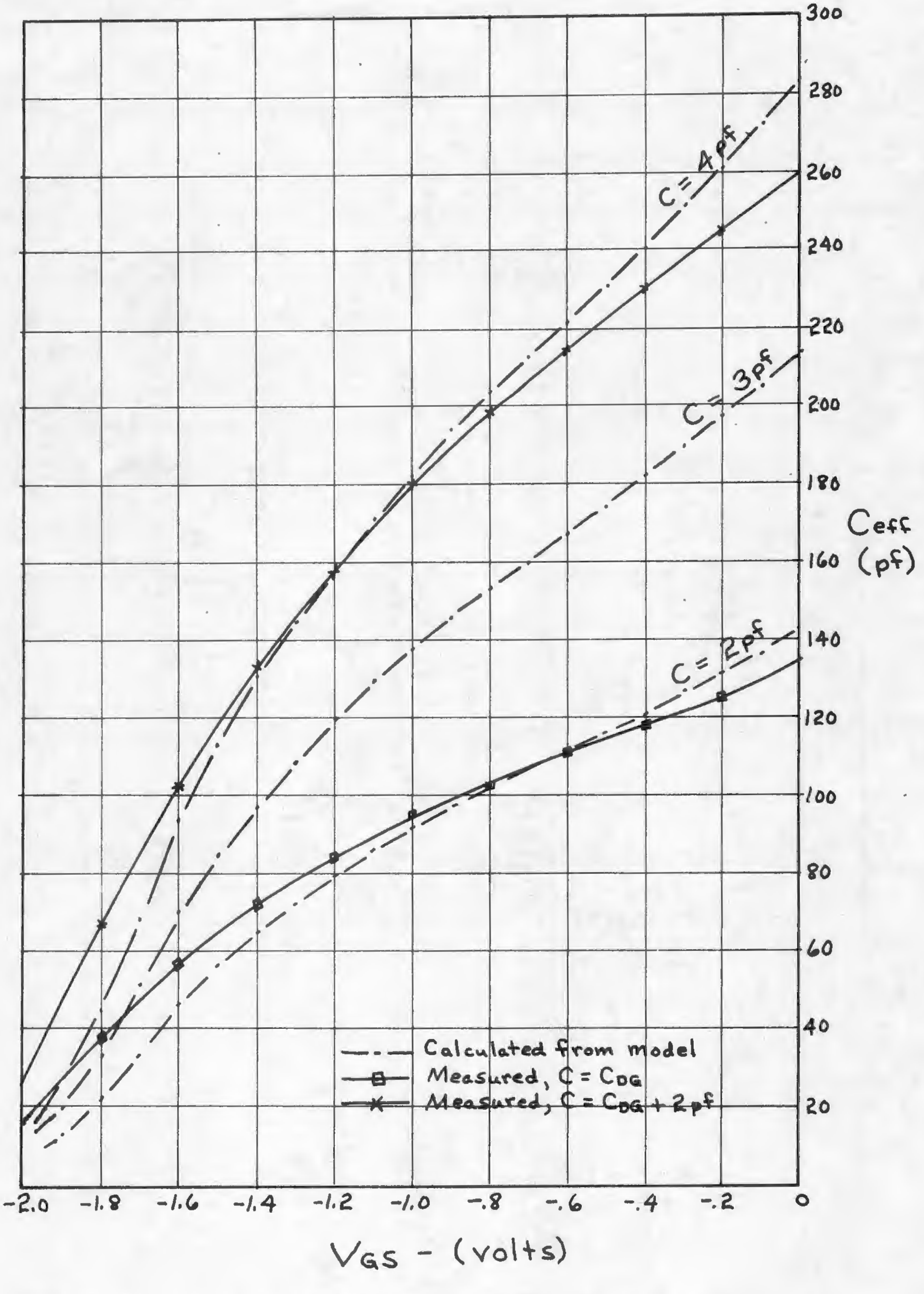


Figure 23. Calculated and measured values of C_{eff} for the simple capacitive reactance circuit of Figure 20.

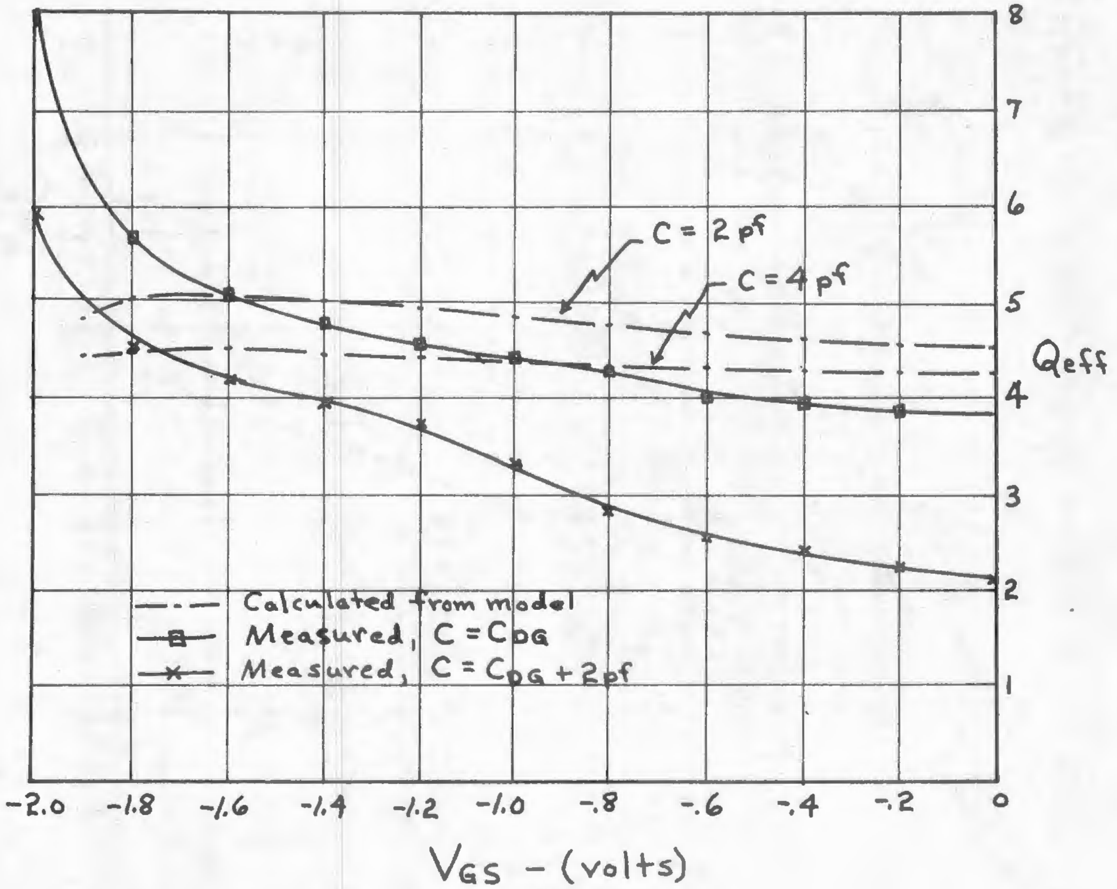


Figure 24. Calculated and measured values of Q_{eff} for the simple capacitive reactance circuit of Figure 20.

C. Capacitive Reactance Circuit with Higher Q

With the values of C_{DG} and C_{SG} for the FET known more accurately, a reactance circuit employing the second-order R-C feedback network, shown in Figure 10(a), was designed.

First, the complex values of v_{gs} and i_1 as functions of R and C were obtained for the bridge network of the feedback path. The computer program of Appendix I was used for these calculations, and besides providing tabulated values of v_{gs} and i_1, a graph showing curves of complex v_{gs} for constant C and varying R was obtained. The tapering parameter m was selected to have a value of one, since the purpose here was to see if a stable, high-Q, effective capacitance could be obtained, and not to design for a particular value of that capacitance. Thus, the bridge network analyzed was that shown in Figure 25, for which the calculated curves of v_{gs}, shown in Figure 26, were obtained.

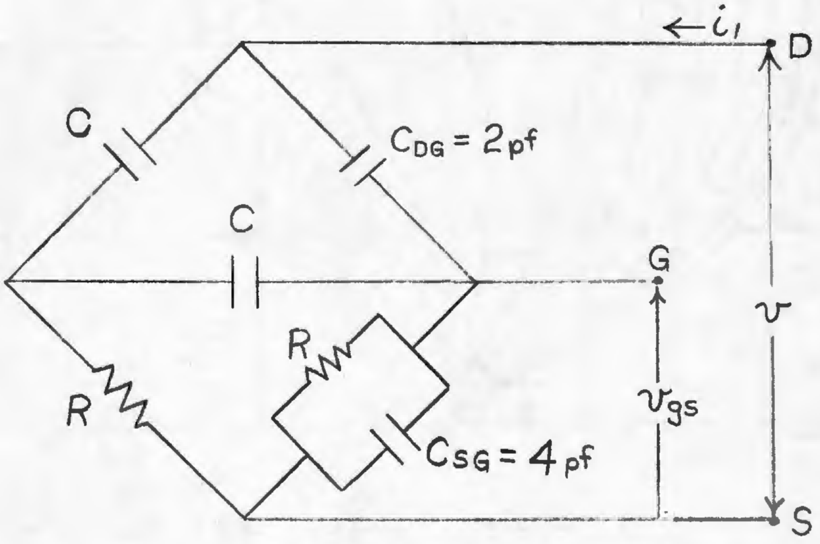


Figure 25. Bridge network used in the design analysis.

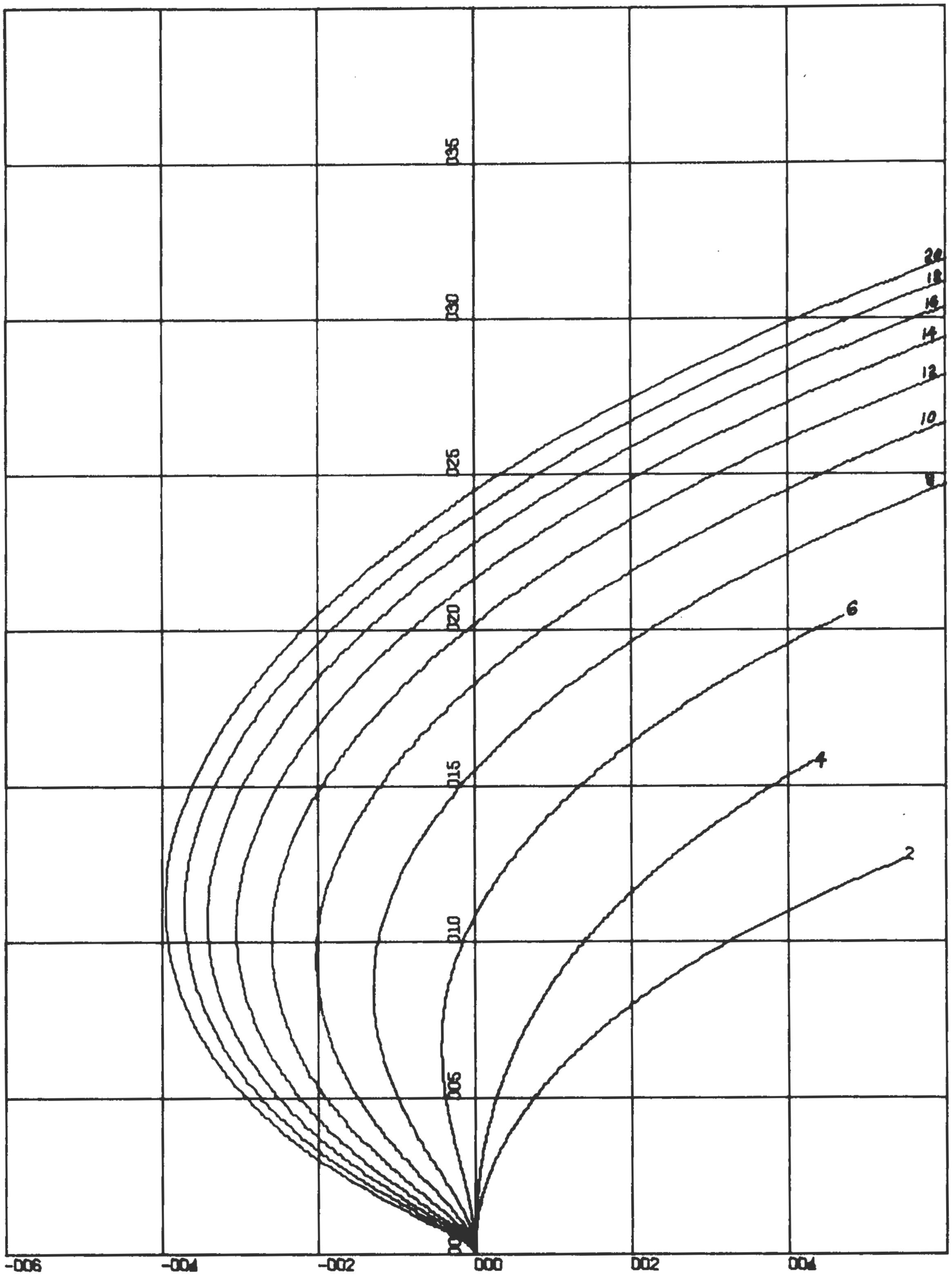


Figure 26. Curves of complex v_{gs} for constant values of C and varying values of R, for the bridge circuit shown in Figure 25, when v is 1.0 volts. Horizontal scale is .03 volts/inch. Vertical scale is 0.5 volts/inch.

In Figure 26, v_{gs} corresponding to R = 0 is at the origin, and for increasing R, the direction of v_{gs} is away from the origin along the curves of constant C. The range of relatively small capacitance was chosen to keep i_1 small. Then, where the $Re(g_m v_{gs})$ is approximately equal in value to g_{DS}, but negative, high values of Q should be obtained.

Using the values of g_m and g_{DS} for $V_{GS} = -1.0$ volts, the above relationship indicates that the $Re(v_{gs})$ should be about -2.6 mv. Where this value occurs along the C = 6 pf curve, appears to be the most stable point, at least for variations in R. The most negative that the $Re(v_{gs})$ becomes along this curve is approximately -4 mv for an R of about 16 KΩ. Rememebring that the measuring circuit to be used includes a standard coil with a finite Q, the reactance circuit could show a negative conductance and still remain stable overall, according to equation (70). In the hope to obtain this effect of Q multiplication, an R of 16 KΩ and a C of 6 pf were chosen.

The capacitive reactance thus fabricated is shown in Figure 27. All of the biasing components, except perhaps the choke coil, have a negligible effect on the dynamic equivalent circuit. The FET was the same one employed previously, and was operated under the same bias conditions, so that the curves of g_m and g_{DS} in Figure 22 were valid.

With the tabulated values of v_{gs} and i_1 substituted into equations (67) and (68), the calculated values of C_{eff}

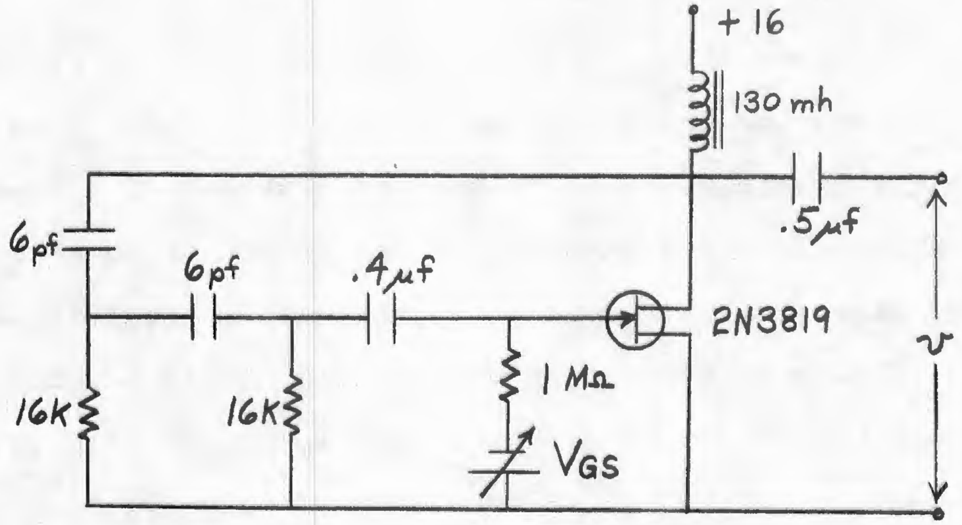


Figure 27. Capacitive reactance circuit providing higher Q.

and Q_{eff} for $V_{GS} = -1.0$ volts were found to be

$$C_{eff} = 114 \text{ pf}$$

$$Q_{eff} = -56$$

Since negative Q values are not usually defined, it is better to express this result in terms of the effective conductance of the circuit, which was found to be

$$G_{eff} = -3.0 \text{ mhos}$$

When measuring the effective Q by the parallel method used previously, applying equation (79) results in a negative value of Q, since $\Delta Q = Q_1 - Q_2$ is negative. Since this result is not considered proper, the following expression which gives G_{eff} in terms of the measured Q and C values was developed from an analysis of the measuring circuit, and applies for both positive and negative conductances.

$$G_{eff} = \frac{\omega C_1 \Delta Q}{Q_1 Q_2} \tag{83}$$

The results of the measurements made on the circuit of Figure 27 are tabulated in Table V. For all of the measurements, the values obtained for C_1 and Q_1 were 398 pf and 174 respectively. The values of C_{eff} and G_{eff} are plotted in Figure 28. It is seen that G_{eff} is negative for V_{GS} in the range of -.9 to -1.7 volts, and it is almost constant in

TABLE V

Measured results for the circuit of Figure 27.

V_{GS} (volts)	C_2 (pf)	Q_2	Q	C_{eff} (pf)	G_{eff} (mhos)
0	201	46	128	197	10.00
-.1	208	53	121	190	8.20
-.2	212	63	111	186	6.34
-.3	218	73	101	180	4.98
-.4	224	84	90	174	3.84
-.5	229	97	77	169	2.86
-.6	235	112	62	163	1.99
-.7	240	130	44	158	1.22
-.8	248	153	21	150	.49
-.9	255	180	-6	143	-.12
-1.0	263	205	-31	135	-.54
-1.1	271	*238	-64	127	-.93
-1.2	276	*282	-108	122	-1.38
-1.3	287	*310	-136	111	-1.58
-1.4	299	*315	-141	99	-1.61
-1.5	310	*300	-126	88	-1.51
-1.6	325	*255	-81	73	-1.14
-1.7	344	*212	-38	54	-.64
-1.8	360	166	8	38	.17
-1.9	375	132	42	23	1.15
-2.0	382	119	55	16	1.65

* Resonance was abrupt when approached from one side, indicating an oscillatory condition not predicted.

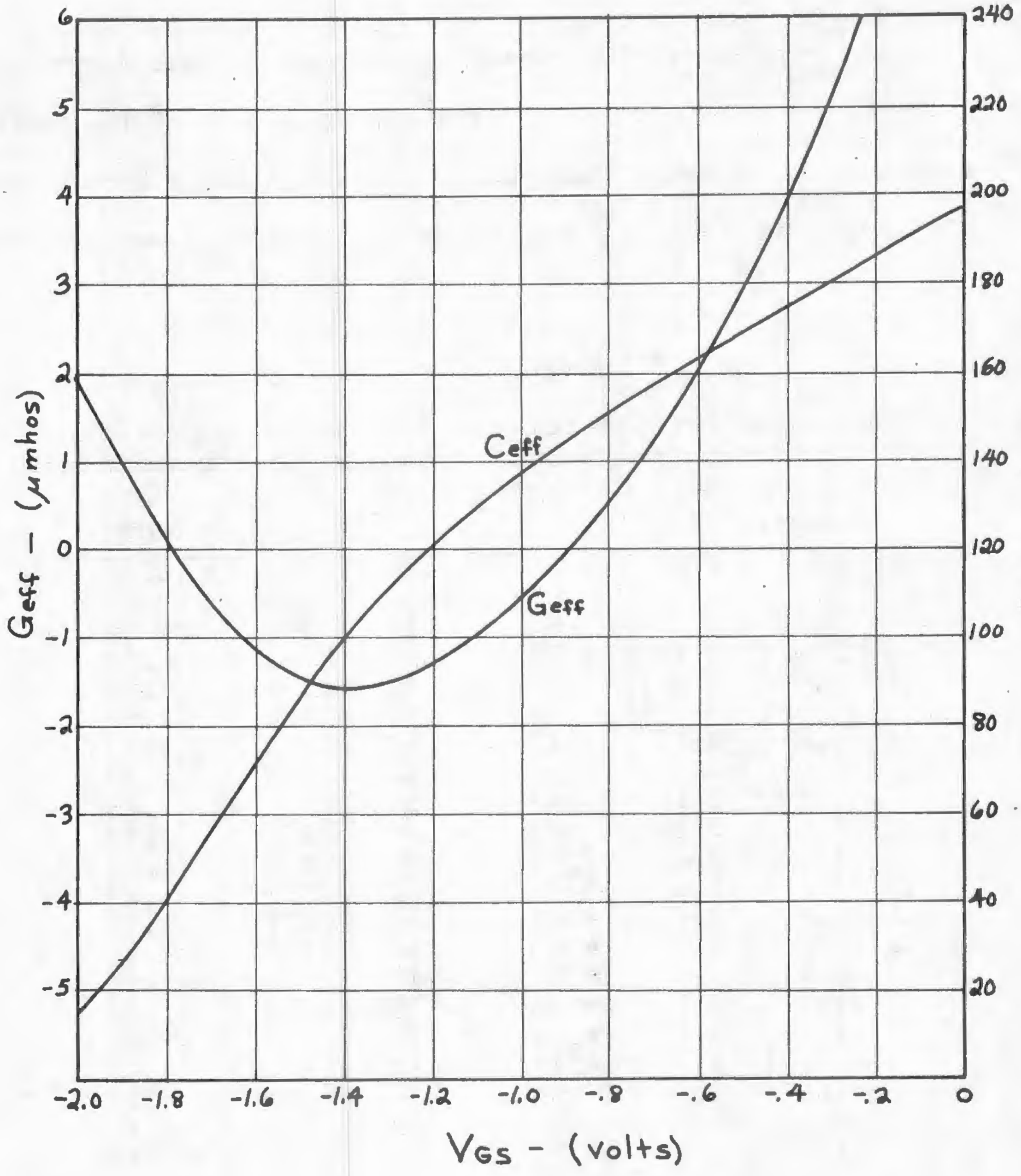


Figure 28. Measured values of C_{eff} and G_{eff} for the capacitive reactance circuit of Figure 27.

the small range from -1.3 to -1.5 volts. In this latter range the capacitance changes by approximately 30 pf; thus a variable capacitive reactance providing an almost constant value of Q multiplication has been achieved. The measured values of C_{eff} and G_{eff} agree quite well with the calculated values considering that the effects of the choke coil were ignored in the calculation.

Because of the existence of a slight instability in the negative conductance region, the circuit was experimentally modified by changing the resistance values. By replacing the fixed resistors with variable ones, the resistance values as shown in Figure 29 were found to produce apparently optimum conditions of stability and Q multiplication for the value of C used.

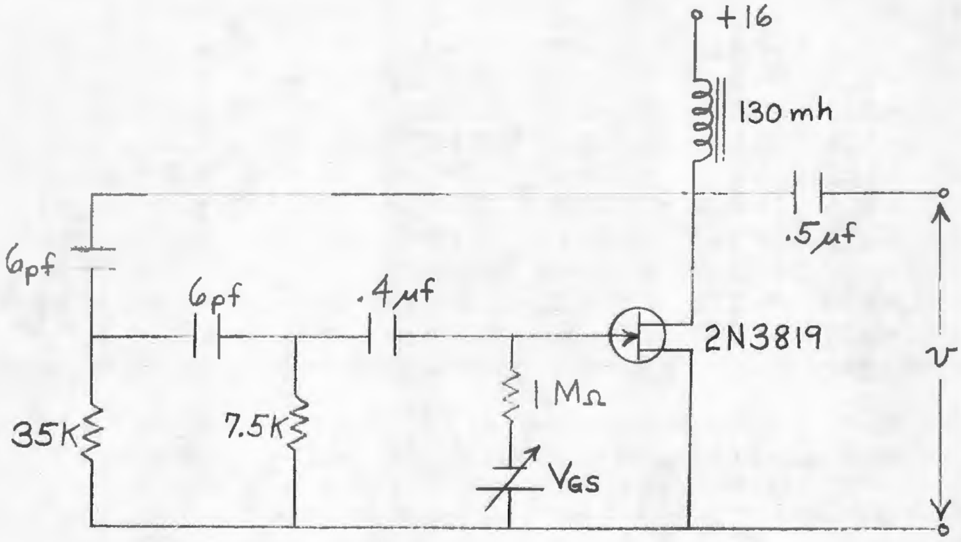


Figure 29. Experimentally modified version of the capacitive reactance circuit shown in Figure 27.

Measurements made on this circuit produced the results tabulated in Table VI and plotted in Figure 30. The curves appear to be horizontally stretched versions of those obtained for the previous circuit. This modification has made the effective capacitance and conductance less sensitive to V_{GS}, and has reduced the range of effective capacitance obtained. However, the magnitude of the negative conductance has been increased, producing greater Q multiplication. When used with an inductor as in the measuring process, the circuit appeared to be completely stable at all times.

TABLE VI

Measured results for the modified reactance circuit of Figure 29. Q_1 = 184, C_1 = 394 pf.

V_{GS} (volts)	C_2 (pf)	Q_2	Q	C_{eff} (pf)	G_{eff} (mhos)
0	272	114	70	122	2.06
-.1	276	132	52	118	1.32
-.2	279	154	30	115	.65
-.3	283	176	8	111	.19
-.4	286	202	-18	108	-.30
-.5	289	236	-52	105	-.74
-.6	292	270	-86	102	-1.07
-.7	296	316	-132	98	-1.41
-.8	300	362	-178	94	-1.66
-.9	304	412	-228	90	-1.86
-1.0	308	462	-278	86	-2.02
-1.1	313	490	-306	81	-2.10
-1.2	318	500	-316	76	-2.12
-1.3	324	490	-306	70	-2.10
-1.4	331	446	-262	63	-1.98
-1.5	339	368	-184	55	-1.68
-1.6	347	290	-106	47	-1.23
-1.7	357	220	-36	37	-.55
-1.8	368	168	16	26	.32
-1.9	378	136	48	16	1.19
-2.0	382	124	60	12	1.63

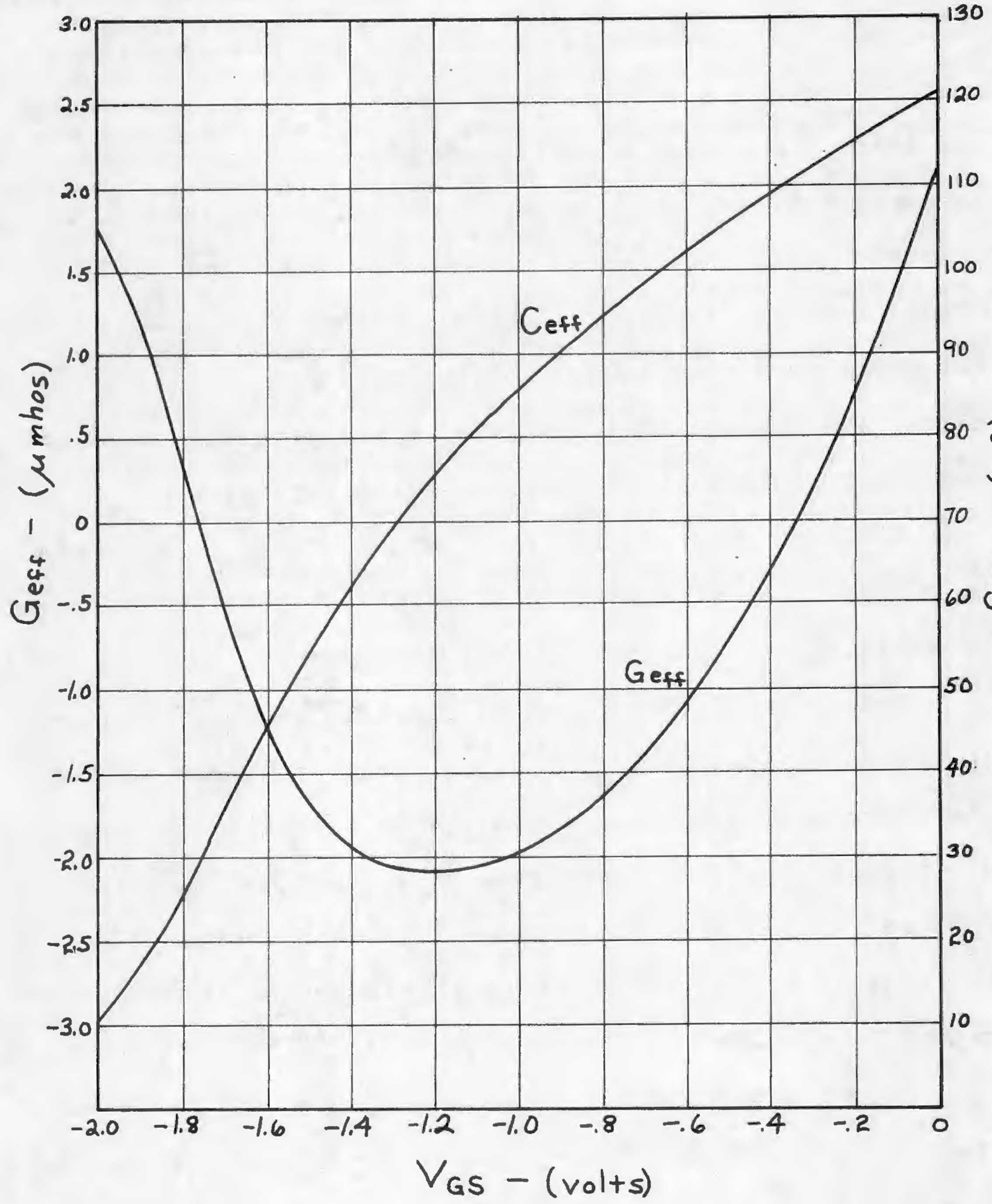


Figure 30. Measured values of C_{eff} and G_{eff} for the capacitive reactance circuit of Figure 29.

When compared to the varactors that were investigated, this capacitive reactance circuit has the distinct advantage of offering Q multiplication as well as a variable capacitance. Although a smaller usable variation in capacitance is obtained, the controlling voltage required is much less than that required to produce the same capacitance change with the varactors. Thus it seems reasonable that FET capacitive reactance circuits, designed by this technique, and appropriately modified experimentally, could be used in certain applications now using varactors.

Although omitted from this report, there is no reason to believe that similar inductive reactance circuits cannot be successfully designed by this same method.

Before these FET reactance circuits can be fabricated in entirely integrated form, some means of biasing without the choke coil must be devised. When a resistor is used, it increases the losses considerably, and thus requires a much larger negative conductance to obtain useful values of Q. This in turn, places closer tolerances on the component values in the feedback network in order to maintain stability. At the present state of the art, it is not believed that the required tolerances can be obtained in integrated circuits.[10] Some other feedback network, either active or passive, might be found which could be successfully integrated with an FET into packaged form.

IV. CONCLUSIONS

The results of the investigation herein reported demonstrate the feasibility of designing an FET reactance circuit to meet rather precise specifications by the use of the equivalent circuit model. The digital computer greatly facilitates design by making possible a rapid evaluation of the modeled circuit over a wide variation of circuit parameters. At the present state of the art, the particular FET reactance circuits investigated are believed to be too sensitive to component tolerances to be packaged in integrated form. However, the design formulae employed in this investigation appear to be valid and point the way to engineering design of even more complicated and sophisticated reactance circuits, one or more of which may prove suitable for packaging in integrated form.

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APPENDIX I

```
C       FEEDBACK NETWORK ANALYSIS FOR CAPACITIVE REACTANCE
C       CIRCUIT
C       CURVES OF VGS IN THE COMPLEX PLANE FOR CONSTANT C
C       AND VARYING R WITH V = 1.0
        DIMENSION X(200), Y(200)
        COMPLEX V, VGS, I1, D, Z1, Z2, Z3, Z4, Z5, Z6, Z7,
       1Z8, Z9
        REAL I1R, I1M
        REAL*8 ITITLE(12)/'CURVES OF COMPLEX VGS FOR CONSTANT
       1 C AND VARYING R - G.D.CLARK - 1968                 '/
        REAL LABEL1/4H2    /,LABEL2/4H    /,LABEL2/4H20  /
      1 READ (5, 100) CDG, CSG, F, M, K
        WRITE (6, 500)
        V1 = 1.0
        WRITE (6, 501)V1, CDG, CSG, F, M
        W = 2.0*F*3.141593
        R = 0.25E 03
        C = 0.2E-11
        Z2 = (0.0,-1.0)/(W*CDG)
        Z6 = (0.0,-1.0)/(W*CSG)
        DO 10 J=1,10
        WRITE (6, 502)
          DO 20 N=1,200
          CC = J*C
          RC = N*R
          Z1 = (0.0,-1.0)/(W*CC)
          Z3 = M*Z1
          Z4 = RC*(1.0,0.0)
          Z5 = M*Z4*Z6/(M*Z4 + Z6)
          Z7 = Z1 + Z4
          Z8 = Z1 + Z2 + Z3
          Z9 = Z3 + Z4 + Z5
          D = Z7*Z8*Z9 - 2.0*Z1*Z3*Z4 - Z8*Z4**2 - Z9*Z1**2
      1   - Z7*Z3**2
          V = V1*(1.0,0.0)
          VGS = V*Z5*(Z1*Z3 + Z4*Z8)/D
          VGSM = CABS(VGS)
          VGSR = REAL(VGS)
          ANGVG = ARCOS(VGSR/VGSM)*180.0/3.141593
          I1 = V*(Z8*Z9 - Z3**2)/D
          I1M = CABS(I1)
          I1R = REAL(I1)
          ANGI1 = ARCOS(I1R/I1M)*180.0/3.141593
          WRITE (6, 503) RC, CC, VGS, VGSM, ANGVG, I1, I1M,
      1   ANGI1
          X(N) = VGSR
          Y(N) = AIMAG(VGS)
     20   CONTINUE
        IF (J .EQ. 1) GO TO 2
        IF (J .EQ. 10) GO TO 3
      CALL DRAW (200,X,Y,2,0,LABEL2,ITITLE,.02,.05,0,3,2,2,
     16,8,1,L)
      GO TO 10
    2 CALL DRAW (200,X,Y,1,0,LABEL1,ITITLE,.02,.05,0,3,2,2,
     16,8,1,L)
      GO TO 10
    3 CALL DRAW (200,X,Y,3,0,LABEL3,ITITLE,.02,.05,0,3,2,2,
     16,8,1,L)
   10 CONTINUE
      IF (K .EQ. 0) GO TO 1
  100 FORMAT (3E15.5, 2I5)
  500 FORMAT (1H1,T8,'V',T20,'CDG',T35,'CSG',T50,'F',T65,
     1'M',/)
  501 FORMAT (1F10.2, 3E15.5,1I10)
  502 FORMAT (//,T8,'R',T20,'C',T37,'VGS',T54,'MAG VGS',
     1T65,'ANGLE VGS',T85,'I1',T102,'MAG I1',T113,'ANGLE I1'
     2,/,T30,'REAL',T42,'IMAG',T78,'REAL',T90,'IMAG',/)
  503 FORMAT (2E12.3, 8F12.6)
      STOP
      END
```

APPENDIX II

```
C      MODEL ANALYSIS - FET REACTANCE TRANSISTOR
       DIMENSION C(3,20), Q(3,20), X(3,20), CO(20), QO(20),
      1VGS(20), GM(20), GDS(20)
       COMPLEX Z1, Z2, Z3, Z4, Z5, Z6, Z7, YOUT
       REAL L
       REAL*8 ITITLE(12)/'MODEL ANALYSIS OF C VS. GATE BIAS
      1   G.D. CLARK                                        '/
       REAL*8 JTITLE(12)/'MODEL ANALYSIS OF Q VS. GATE BIAS
      1   G.D. CLARK                                        '/
       REAL*8 LABEL1/8HC    2   /,LABEL2/8HC    3   /,LABEL3/
      18HC    4   /,LABEL4/8HQ    2   /,LABEL5/8HQ    3   /,
      2LABEL6/8HQ    4   /
     1 READ (5, 100) R, CSG, L, F, K
       WRITE (6, 200)
       WRITE (6, 201) R, CGS, L, F
       W = 2.0*F*3.141593
       Z4 = (0.0,-1.0)/(W*CSG)
       Z5 = (1.0,0.0)*R
       Z2 = Z4*Z5/(Z4 + Z5)
       Z6 = W*L*(0.0,1.0)
       DO 5 I=1,20
     5   READ (5, 101) VGS(I), GM(I), GDS(I)
       DO 10 J=2,4
         CDG = J*0.1E-11
         Z1 = (0.0,-1.0)/(W*CDG)
         WRITE (6, 202) CDG
         DO 20 N=1,20
           Z7 = (1.0,0.0)/GDS(N)
           Z3 = Z6*Z7/(Z6 + Z7)
           YOUT = (GM(N)*Z2 + 1.0)/(Z1 + Z2) + 1.0/Z3
           BO = AIMAG(YOUT)
           GO = REAL(YOUT)
           CEFF = BO/W
           QEFF = BO/GO
           C(J,N) = CEFF
           Q(J,N) = QEFF
           X(J,N) = VGS(N)
           WRITE (6, 203) GM(N), GDS(N), VGS(N), GO, BO,
      1    CEFF, QEFF
    20   CONTINUE
    10 CONTINUE
        DO 30 J=2,4
          DO 40 N=1,20
            XO(N) = X(J,N)
            CO(N) = C(J,N)
    40    CONTINUE
          IF (J .EQ. 2) GO TO 31
          IF (J .EQ. 4) GO TO 32
          CALL DRAW (20,XO,CO,2,2,LABEL2,ITITLE,.3,.2E-10,0,
      1   7,2,2,7,15,1,L)
          GO TO 30
```

```
 31    CALL DRAW (20,XO,CO,1,1,LABEL1,ITITLE,.3,.2E-10,0,
   1   7,2,2,7,15,1,L)
       GO TO 30
 32    CALL DRAW (20,XO,CO,3,3,LABEL3,ITITLE,.3,.2E-10,0,
   1   7,2,2,7,15,1,L)
 30  CONTINUE
     DO 50 J=2,4
       DO 60 N=1,20
         XO(N) = X(J,N)
         QO(N) = Q(J,N)
 60    CONTINUE
       IF (J .EQ. 2) GO TO 51
       IF (J .EQ. 4) GO TO 52
       CALL DRAW (20,XO,QO,2,2,LABEL5,JTITLE,.3,1.,0,7,2,
   1   2,7,10,1,L)
       GO TO 50
 51    CALL DRAW (20,XO,QO,1,1,LABEL4,JTITLE,.3,1.,0,7,2,
   1   2,7,10,1,L)
       GO TO 50
 52    CALL DRAW (20,XO,QO,3,3,LABEL6,JTITLE,.3,1.,0,7,2,
   1   2,7,10,1,L)
 50  CONTINUE
     IF (K .EQ. 0) GO TO 1
100  FORMAT (4E10.3, I5)
101  FORMAT (1F10.1, 2E10.3)
200  FORMAT (1H1,T10,'R',T25,'CSG',T40,'L',T55,'F',/)
201  FORMAT (4E15.5)
202  FORMAT (/,T9,'CDG =',1E10.3,//,T10,'GM',T25,'GDS',
    1T40,'VGS',T55,'GO',T70,'BO',T85,'CEFF',T100,'QEFF',/)
203  FORMAT (7E15.5)
     STOP
     END
```

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13. ABSTRACT

Efforts to miniaturize the reactance circuits of vacuum-tube technology by using junction transistors have been only partially successful. Large equivalent inductances and capacitances are obtainable, but the effective Q is limited to low values by the low input impedance of these devices. Unipolar field-effect transistors offering high gain and high input impedance are investigated for this application. Analytical models, based on the equivalent circuit of the FET, are developed for reactance circuits employing R-C feedback networks. A simple capacitive reactance circuit, utilizing a first-order feedback network and operating at a frequency of 250 KHz, yielded a low-Q effective capacitance but served to verify the model emplyed. Computer-aided design of a reactance circuit employing a second-order feedback network resulted in a stable effective capacitance offering Q multiplication. Sensitivity of the feedback voltage to component tolerances precludes packaging this circuit in integrated form, but the feasibility of designing an FET reactance circuit to meet rather precise specifications is demonstrated.

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